DATASHEET

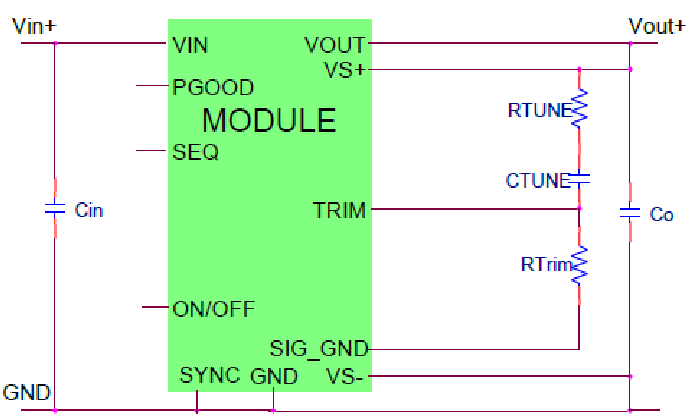
12A Analog Pico SlimLynx™ Open Frame: Non-Isolated DC-DC Modules

$3V_{dc}$ –$14.4V_{dc}$ input; $0.6V_{dc}$ to $5.5V_{dc}$ output; 12A Output Current

RoHS Compliant

Description

The 12A Analog Pico SlimLynx™ Open Frame power modules are non-isolated dc-dc converters that can deliver up to 12A of output current. These modules operate over a wide range of input voltage (V_{IN} = $3V_{dc}$-$14.4V_{dc}$) and provide a precisely regulated output voltage from $0.6V_{dc}$ to $5.5V_{dc}$, programmable via an external resistor. Features include remote On/Off, adjustable output voltage, over current and over temperature protection. The module also includes the Tunable Loop™ feature that allows the user to optimize the dynamic response of the converter to match the load with reduced amount of output capacitance leading to savings on cost and PWB area.



Applications

- Distributed power architectures
- Intermediate bus voltage applications
- Telecommunications equipment
- Servers and storage applications
- Networking equipment
- Industrial equipment

See footnotes on page 2

Features

- Compliant to RoHS II EU "Directive 2011/65/EU" and amended Directive (EU) 2015/863
- Compliant to REACH Directive (EC) No 1907/2006
- Compliant to IPC-9592 (September 2008), Category 2, Class II
- Ultra low height design for very dense power applications.
- Small size: 12.2 mm x 12.2 mm x 2.9 mm (Max) (0.48 in x 0.48 in x 0.116 in)
- Output voltage programmable from 0.6V_{dc} to 5.5V_{dc} via external resistor.
- Wide Input voltage range (3V_{dc}-14.4V_{dc})
- Wide operating temperature range [-40°C to 85°C]. See derating curves
- DOSA approved footprint
- Tunable Loop™ to optimize dynamic output voltage response
- Flexible output voltage sequencing EZ-SEQUENCE
- Power Good signal
- Remote On/Off
- Fixed switching frequency with capability of external synchronization
- Output overcurrent protection (non-latching)
- Overtemperature protection
- Ability to sink and source current
- Compatible in a Pb-free or SnPb reflow environment
- ANSI/UL* 62368-1 and CAN/CSA† C22.2 No. 62368-1 Recognized, DIN VDE‡ 0868-1/A11:2017 (EN62368- 1:2014/A11:2017)
- ISO** 9001 and ISO 14001 certified manufacturing facilities

FOOTNOTES

*UL is a registered trademark of Underwriters Laboratories, Inc.

†CSA is a registered trademark of Canadian Standards Association.

‡VDE is a trademark of Verband Deutscher Elektrotechniker e.V.

**ISO is a registered trademark of the International Organization of Standards

Technical Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Device	Symbol	Min	Max	Unit
Input Voltage Continuous	All	V_{IN}	-0.3	15	V
SEQ, SYNC, VS+	All			7	V
Operating Ambient Temperature (see Thermal Considerations section)	All	T_A	-40	85	°C
Storage Temperature	All	T_{stg}	-55	125	°C

Electrical Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions.

Parameter	Device	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	All	V_{IN}	3	—	14.4	V_{dc}
Maximum Input Current (V_{IN} =3V to 14V, I_O =$I_{O, max}$)	All	$I_{IN,max}$			11	A_{dc}
Input No Load Current (V_{IN} = 12V_{dc}, I_O = 0, module enabled)	$V_{O,set}$ = 0.6 V_{dc}	$I_{IN,No\ load}$		50		mA
	$V_{O,set}$ = 5.5V_{dc}	$I_{IN,No\ load}$		180		mA
Input Stand-by Current (V_{IN} = 12V_{dc}, module disabled)	All	$I_{IN,stand\text{-}by}$		8		mA
Inrush Transient	All	I^2t			1	A^2s
Input Reflected Ripple Current, peak-to-peak (5Hz to 20MHz, 1μH source impedance; V_{IN} =0 to 14V, I_O=$I_{O, max}$; See Test Configurations)	All			30		mA_{p-p}
Input Ripple Rejection (120Hz)	All			-55		dB
Output Voltage Set-point (with 0.1% tolerance for external resistor used to set output voltage)	All	$V_{O, set}$	-1.0		+1.0	% $V_{O, set}$
Output Voltage (Over all operating input voltage, resistive load, and temperature conditions until end of life)	All	$V_{O, set}$	-3.0	—	+3.0	% $V_{O, set}$
Adjustment Range (selected by an external resistor) (Some output voltages may not be possible depending on the input voltage – see Feature Descriptions Section)	All	V_O	0.6		5.5	V_{dc}
Remote Sense Range	All				0.5	V_{dc}
Output Regulation (for $V_O \geq 2.5V_{dc}$)						
Line (V_{IN}=V_{IN}, min to V_{IN}, max)	All			—	+0.4	% $V_{O, set}$
Load (I_O=$I_{O, min}$ to $I_{O, max}$)	All			—	10	mV
Output Regulation (for $V_O < 2.5V_{dc}$)						
Line (V_{IN}=$V_{IN, min}$ to $V_{IN, max}$)	All			—	5	mV
Load (I_O=$I_{O, min}$ to $I_{O, max}$)	All			—	10	mV
Temperature (T_{ref}=$T_{A, min}$ to $T_{A, max}$)	All			—	0.4	% $V_{O, set}$
Input Noise on nominal input at 25°C (V_{IN}=$V_{IN, nom}$ and I_O=$I_{O, min}$ to $I_{O, max}$ C_{in} = 1x47nF(0402) or equivalent , 2x22uF(1210) ceramic capacitors or equivalent and Peak-to-Peak (Full Bandwidth) for all V_o	All		-	360		mA_{p-kpk}

Technical Specifications (continued)

Electrical Specifications (continued)

Parameter	Device	Symbol	Min	Typ	Max	Unit
Output Ripple and Noise on nominal output at 25°C (V_{IN}=$V_{IN, nom}$ and I_O=$I_{O, min}$ to $I_{O, max}$ C_o = 2x47nF(0402) or equivalent,2x47uF (1210) or equivalent ceramic capacitors on output and 1x47nF(0402) or equivalent, 2x22uF(1210) ceramic capacitors or equivalent and 470uF,16V electrolytic) on input						
Peak-to-Peak (Full bandwidth) Vo≤1.2V_o				30		mV_{pk-pk}
Peak-to-Peak (Full bandwidth) Vo>1.2V_o	All			3%Vo		mV_{pk-pk}
RMS (Full bandwidth) for all V_o	All			2%Vo		mV_{rms}
External Capacitance[1]						
Without the Tunable Loop™						
ESR ≥ 1 mΩ	All	$C_{O, max}$	1x47μF		200μF	μF
With the Tunable Loop™						
ESR ≥ 0.15 mΩ	All	$C_{O, max}$	200		1000	μF
ESR ≥ 10 mΩ	All	$C_{O, max}$			5000	μF
Output Current (in either sink or source mode)	All	I_o	0		12	A_{dc}
Output Current Limit Inception (Hiccup Mode) (current limit does not operate in sink mode)	All	$I_{O, lim}$		130		% $I_{o,max}$
Output Short-Circuit Current (V_O≤250mV) (Hiccup Mode)	All	$I_{O, s/c}$		1.3		A_{rms}
Efficiency	$V_{O,set}$ = 0.6V_{dc}	η		70.8		%
V_{IN}= 12V_{dc}, T_A=25°C	$V_{O,set}$ = 1.2V_{dc}	η		81.5		%
I_O=$I_{O, max}$, V_O= $V_{O,set}$	$V_{O,set}$ = 1.8V_{dc}	η		85.7		%
	$V_{O,set}$ = 2.5V_{dc}	η		88.3		%
	$V_{O,set}$ = 3.3V_{dc}	η		90.1		%
	$V_{O,set}$ = 5.0V_{dc}	η		92.5		%
Switching Frequency	All	f_{sw}	—	800	—	kHz
Frequency Synchronization	All					
Synchronization Frequency Range	All		760	800	840	kHz
High-Level Input Voltage	All	V_{IH}	2			V
Low-Level Input Voltage	All	V_{IL}			0.4	V
Input Current, SYNC	All	I_{SYNC}			100	nA
Minimum Pulse Width, SYNC	All	t_{SYNC}	100			ns
Maximum SYNC rise time	All	t_{SYNC_SH}	100			ns

[1] External capacitors may require using the new Tunable Loop™ feature to ensure that the module is stable as well as getting the best transient response. See the Tunable Loop™ section for details.

General Specifications

Parameter	Device	Min	Typ	Max	Unit
Calculated MTBF (I_O=0.8$I_{O, max}$, T_A=40°C) Telcordia Issue 3 Method 1 Case 3	All		29,951,054		Hours
Weight		—	0.732	—	g (oz.)

Technical Specifications (continued)

Feature Specifications

Unless otherwise indicated, specifications apply overall operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information.

Parameter	Device	Symbol	Min	Typ	Max	Unit
On/Off Signal Interface (V_{IN}=$V_{IN, min}$ to $V_{IN, max}$; open collector or equivalent, Signal referenced to GND) Device Code with no suffix – Negative Logic (See Ordering Information) (On/OFF pin is open collector/drain logic input with external pull-up resistor; signal referenced to GND)						
Logic High (Module OFF)						
Input High Current	All	I_{IH}	—	—	1	mA
Input High Voltage	All	V_{IH}	2	—	$V_{IN, max}$	V_{dc}
Logic Low (Module ON)						
Input low Current	All	I_{IL}	—	—	50	µA
Input Low Voltage	All	V_{IL}	-0.2	—	0.6	V_{dc}
Turn-On Delay and Rise Times						
(V_{IN}=$V_{IN, nom}$, I_O=$I_{O, max}$, V_O to within ±1% of steady state)						
Case 1: On/Off input is enabled and then input power is applied (delay from instant at which V_{IN} = $V_{IN, min}$ until V_o =10% of $V_{o, set}$)	All	T_{delay}	—	0.9	—	msec
Case 2: Input power is applied for at least one second and then the On/Off input is enabled (delay from instant at which Von/Off is enabled until V_o = 10% of $V_{o, set}$)	All	T_{delay}	—	0.8	—	msec
Output voltage Rise time(time for V_o to rise from 10% of $V_{o, set}$ to 90% of $V_{o, set}$)	All	T_{rise}	—	2	—	msec
Output voltage overshoot (T_A = 25°C V_{IN}= $V_{IN, min}$ to $V_{IN, max}$,I_O = $I_{O, min}$ to $I_{O, max}$) With or without maximum external capacitance					3	% $V_{O, set}$
Over Temperature Protection (See Thermal Considerations section)	All	T_{ref}		130		°C
Tracking Accuracy (Power-Up: 2V/ms)	All	V_{SEQ} –V_o		100		mV
(Power-Down: 2V/ms) ($V_{IN, min}$ to $V_{IN, max}$; $I_{O, min}$ to $I_{O, max}$ V_{SEQ} < Vo)	All	V_{SEQ} –V_o		100		mV
Input Undervoltage LOCKOUT						
Turn-off Threshold	All			3		V_{dc}
Turn-off Threshold	All			2.75		V_{dc}
Hysteresis	All			0.25		V_{dc}
PGOOD (Power Good)						
Signal Interface Open Drain, V_{supply} ≤ 5V_{DC}						
Overvoltage threshold for PGOOD ON	All			108		%$V_{O, set}$
Overvoltage threshold for PGOOD OFF	All			110		%$V_{O, set}$
Undervoltage threshold for PGOOD ON	All			92		%$V_{O, set}$
Undervoltage threshold for PGOOD OFF	All			90		%$V_{O, set}$
Pulldown resistance of PGOOD pin	All				50	Ω
Sink current capability into PGOOD pin	All				5	mA

Technical Specifications (continued)

Characteristic Curves

The following figures provide typical characteristics for the 12A Analog Pico SlimLynx™ at 0.6V$_o$ and 25°C.

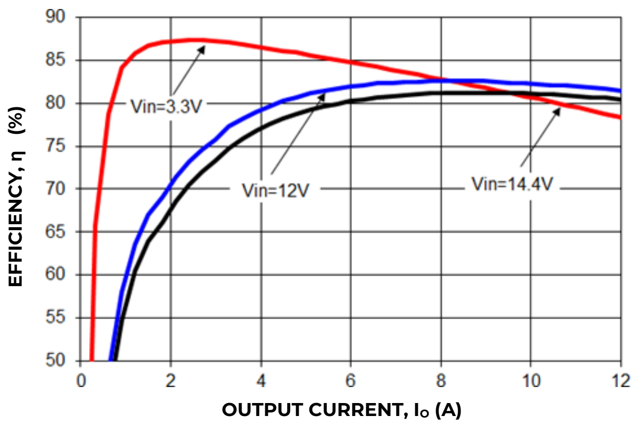


Figure 1. Converter Efficiency verses output current

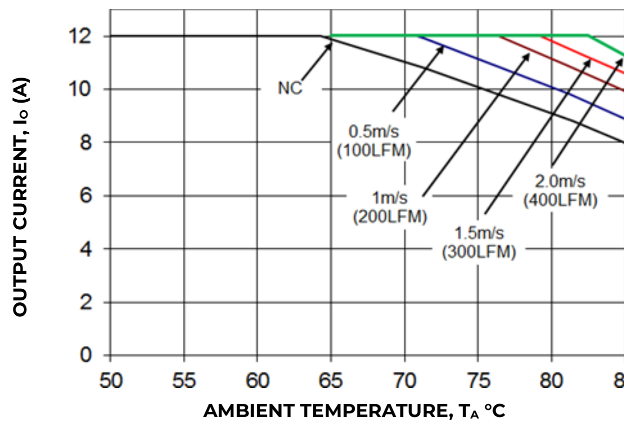


Figure 2. Derating Output Current verses Ambient Temperature and Airflow.

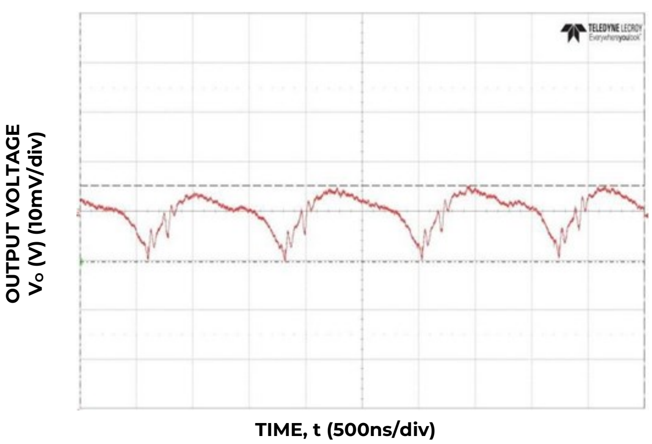


Figure 3. Typical output ripple
(C_O=2x47μF ceramic, V_{IN} = 12V, I_o = $I_{o,max,}$ 20MHz BW).

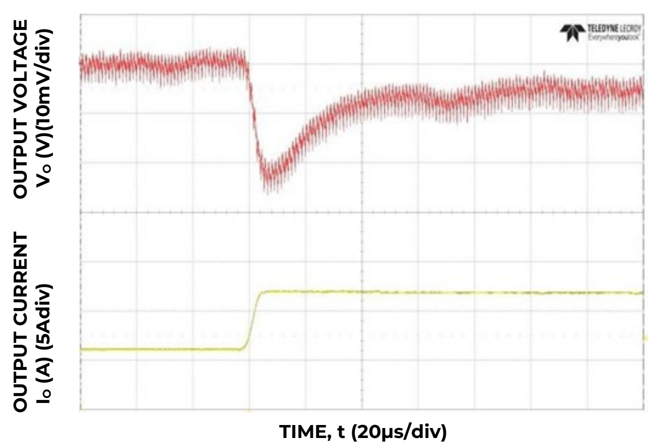


Figure 4. Transient Response to Dynamic Load Change from 50% to 100% at 12V$_{in}$, C_{out}= 4x47uF + 6x330uF, C_{Tune}=47nF, R_{Tune}=300

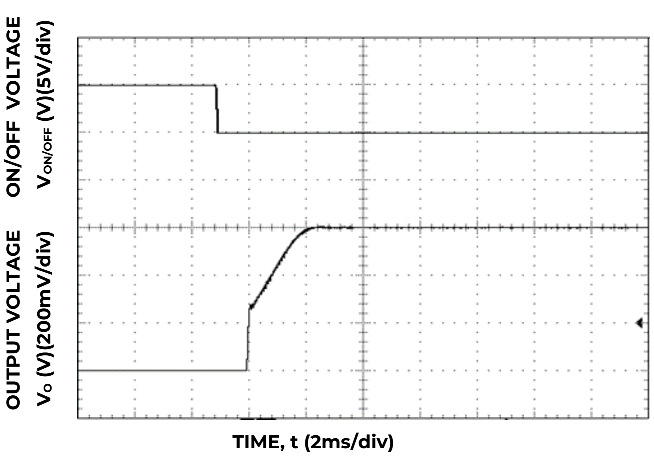


Figure 5. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

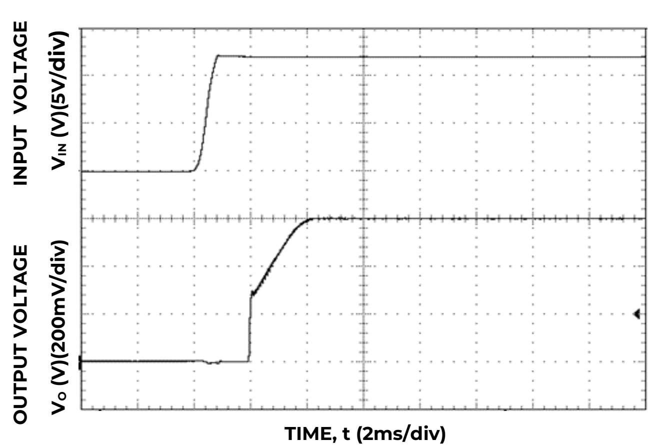


Figure 6. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

Technical Specifications (continued)

Characteristic Curves (continued)

The following figures provide typical characteristics for the 12A Analog Pico SlimLynx™ at 1.2V$_o$ and 25°C.

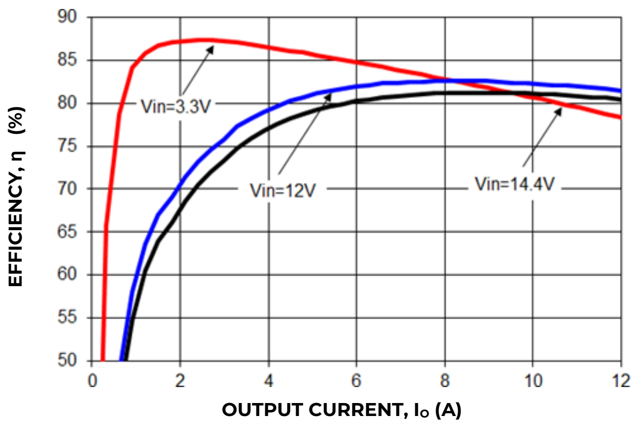


Figure 7. Converter Efficiency versus Output Current.

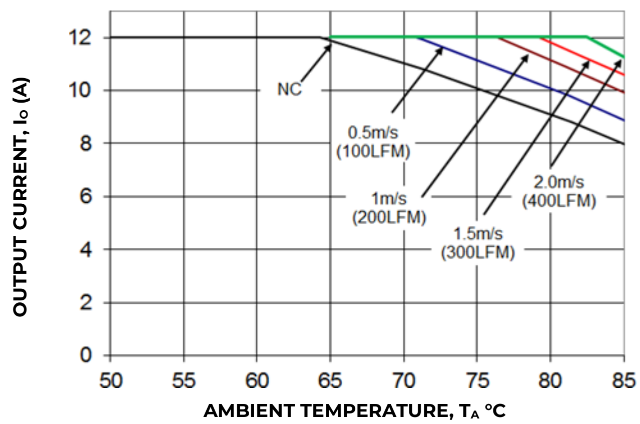


Figure 8. Derating Output Current versus Ambient Temperature and Airflow.

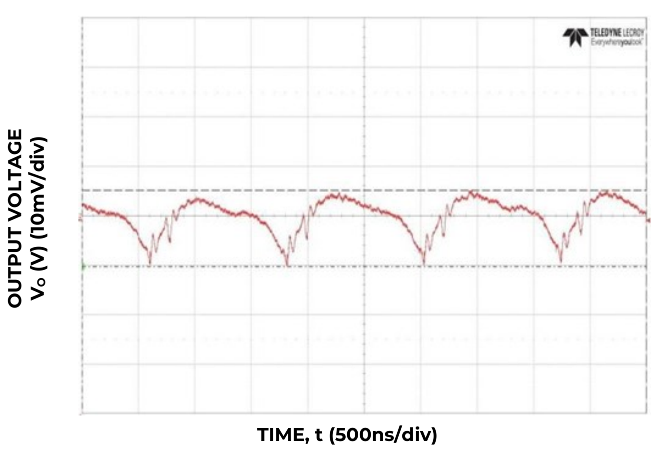


Figure 9. Typical output ripple (C_O=2x47µF ceramic, VIN = 12V, $I_{o=I_{o,max}}$, 20MHz BW).

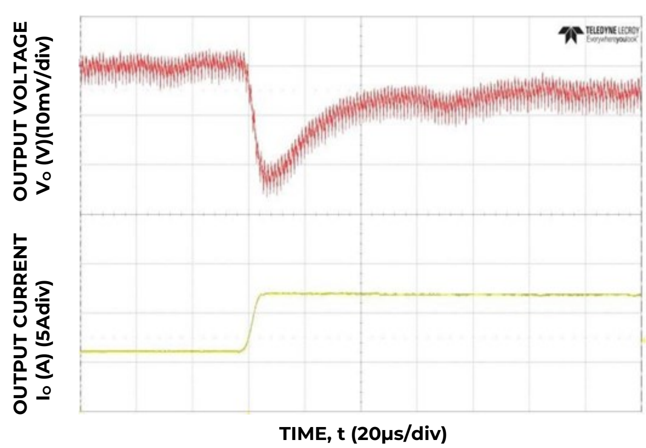


Figure 10. Transient Response to Dynamic Load Change from 50% to 100% at 12V$_{in}$, C_{out}=4x47uF+3x330uF, C_{Tune}=10nF, R_{Tune}=300

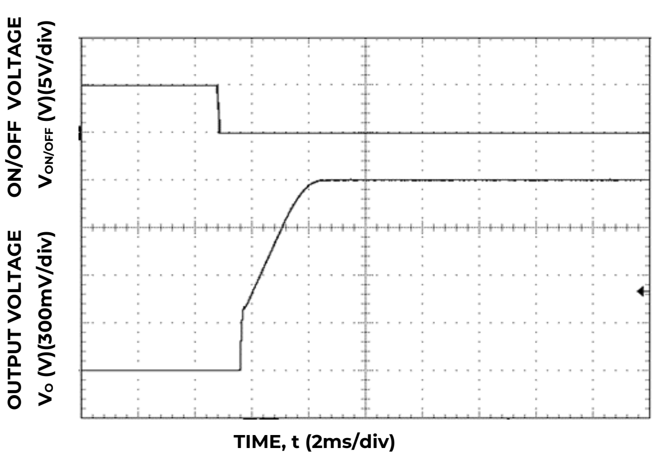


Figure 11. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

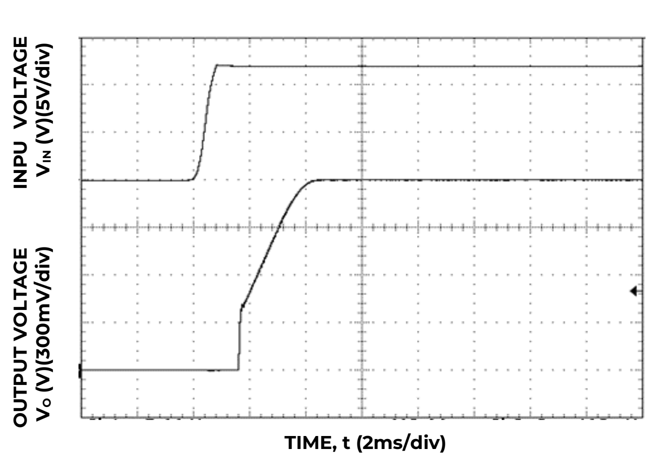


Figure 12. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o =$I_{o,max}$).

Technical Specifications (continued)

Characteristic Curves (continued)

The following figures provide typical characteristics for the 12A Analog Pico SlimLynx™ at 1.8V$_o$ and 25°C.

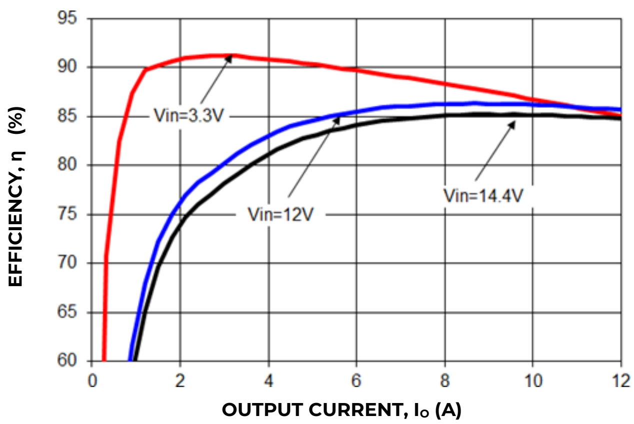


Figure 13. Converter Efficiency versus Output Current.

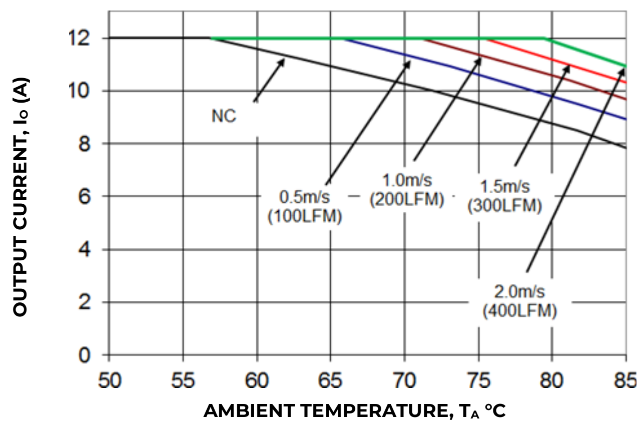


Figure 14. Derating Output Current versus Ambient Temperature and Airflow..

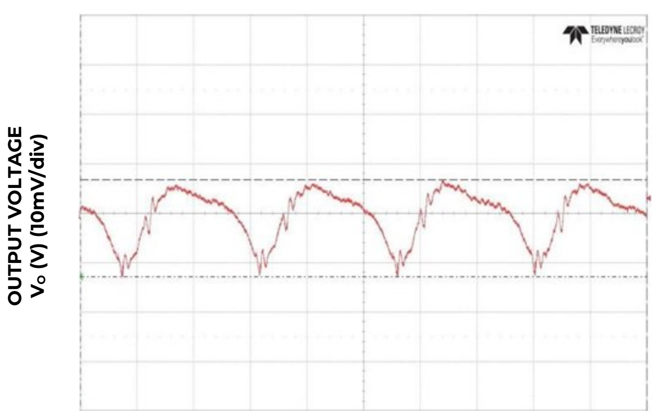


Figure 15. Typical output ripple (C$_O$=2x47μF ceramic, V$_{IN}$ = 12V, I$_o$ = I$_{o,max}$, 20MHz BW).

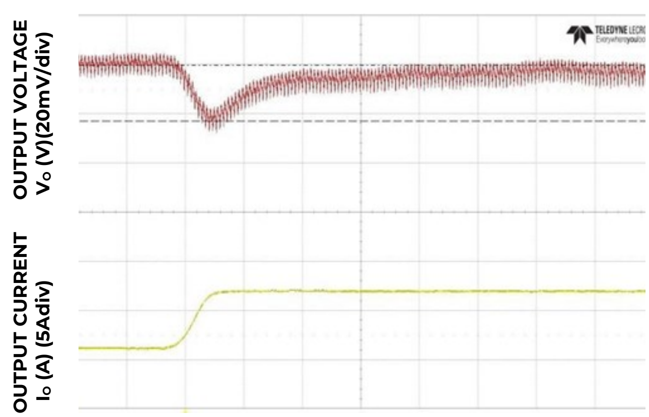


Figure 16. Transient Response to Dynamic Load Change from 50% to 100% at 12V$_{in}$, C$_{out}$=4x47uF+2x330uF, C$_{Tune}$=8.2nF, R$_{Tune}$=300

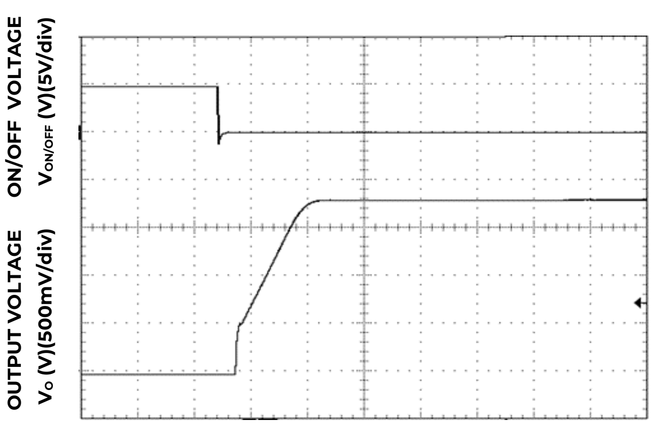


Figure 17. Typical Start-up Using On/Off Voltage (I$_o$ = I$_{o,max}$).

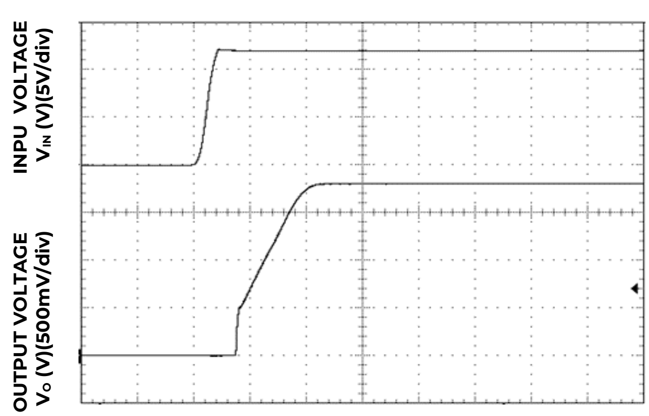


Figure 18. Typical Start-up Using Input Voltage (V$_{IN}$ = 12V, I$_o$ =I $_{o,max}$).

Technical Specifications (continued)

Characteristic Curves (continued)

The following figures provide typical characteristics for the 12A Analog Pico SlimLynx™ at 2.5V$_o$ and 25°C.

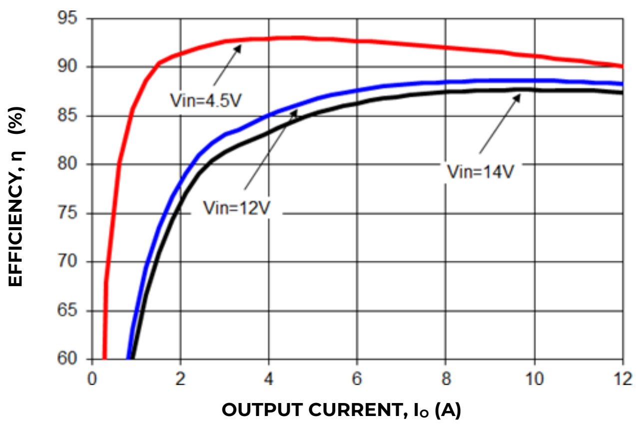


Figure 19. Converter Efficiency versus Output Current.

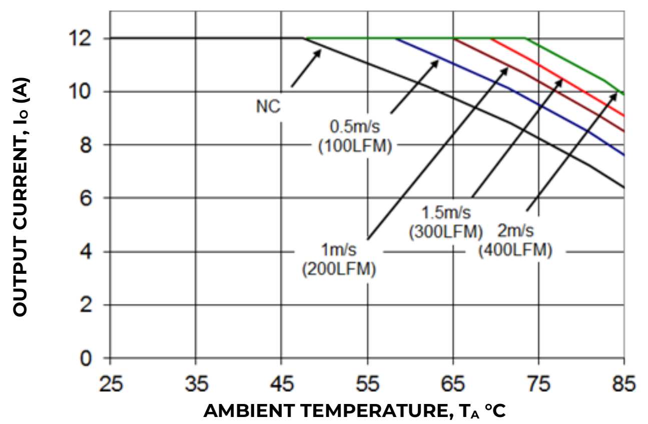


Figure 20. Derating Output Current versus Ambient Temperature and Airflow..

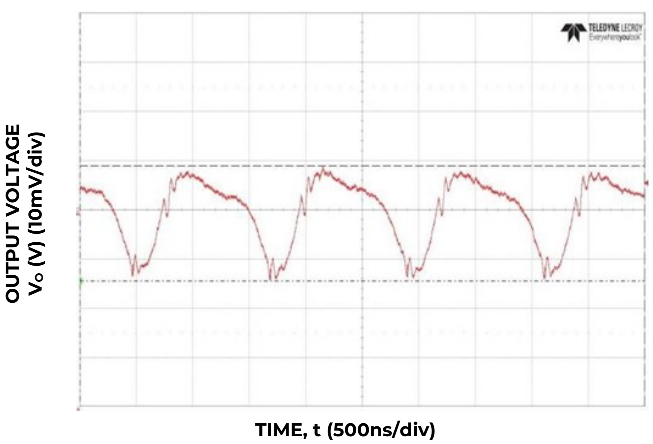


Figure 21. Typical output ripple (C_O=2x47µF ceramic, V_{IN} = 12V, $I_o = I_{o,max}$, 20MHz BW).

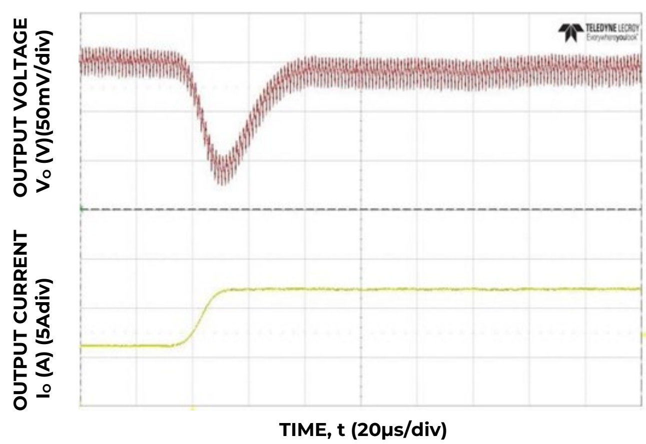


Figure 22. Transient Response to Dynamic Load Change from 50% to 100% at 12V$_{in}$, C_{out}=4x47uF+1x330uF, C_{Tune}=2700p, R_{Tune}=300

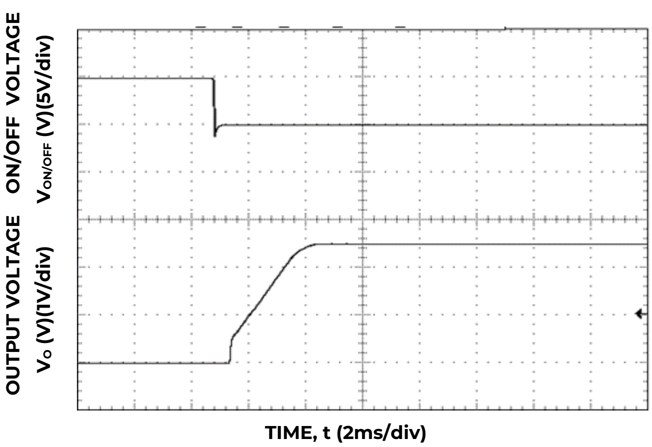


Figure 23. Typical Start-up Using On/Off Voltage ($I_o = I_{o,max}$).

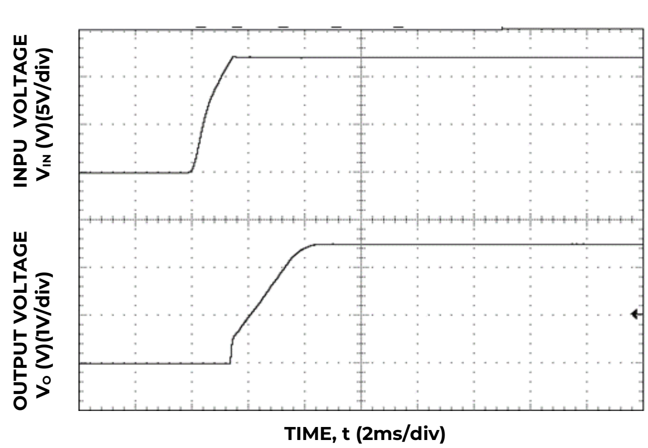


Figure 24. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o=$I_{o,max}$).

Technical Specifications (continued)

Characteristic Curves (continued)

The following figures provide typical characteristics for the 12A Analog Pico SlimLynx™ at 3.3V_o and 25°C.

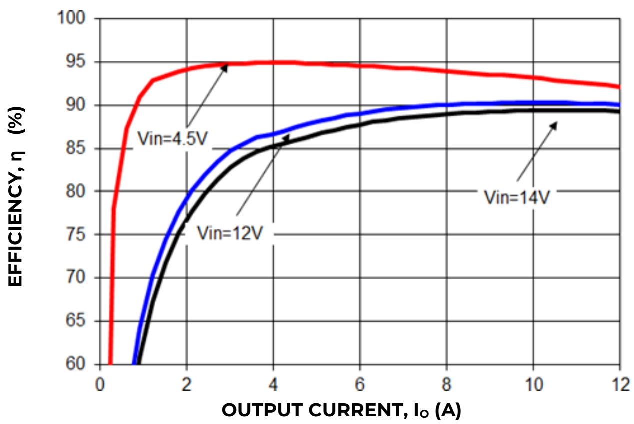


Figure 25. Converter Efficiency versus Output Current.

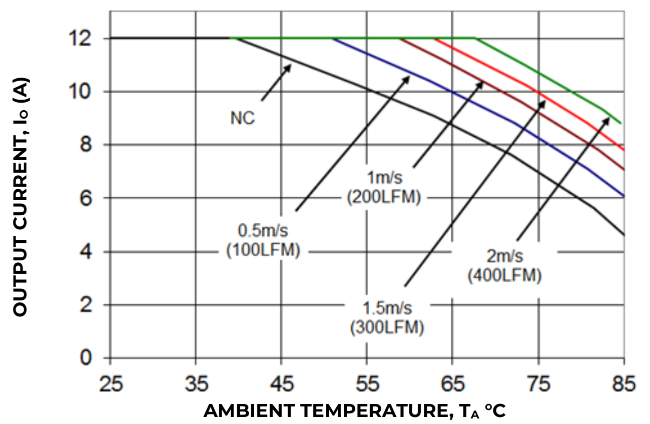


Figure 26. Derating Output Current versus Ambient Temperature and Airflow..

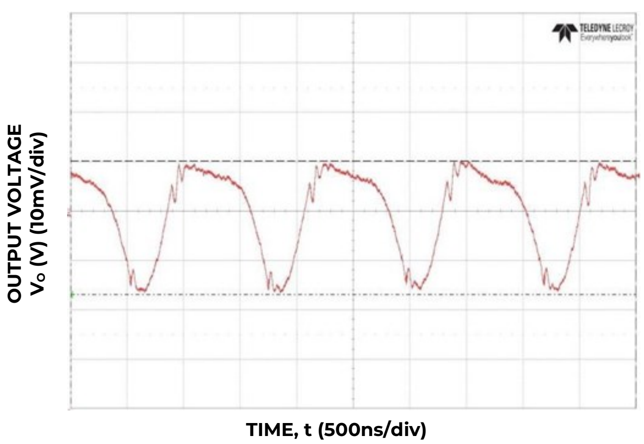


Figure 27. Typical output ripple (C_O=2x47µF ceramic, V_{IN} = 12V, I_o = $I_{o,max}$, 20MHz BW).

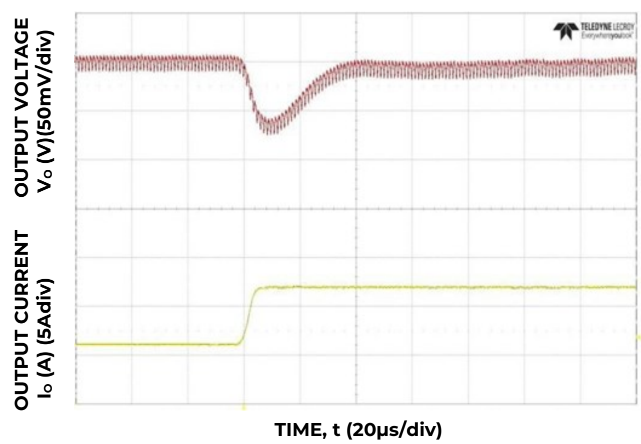


Figure 28. Transient Response to Dynamic Load Change from 50% to 100% at 12V_{in}, C_{out}=3x47uF+1x330uF, C_{Tune}=1800pF, R_{Tune}=300

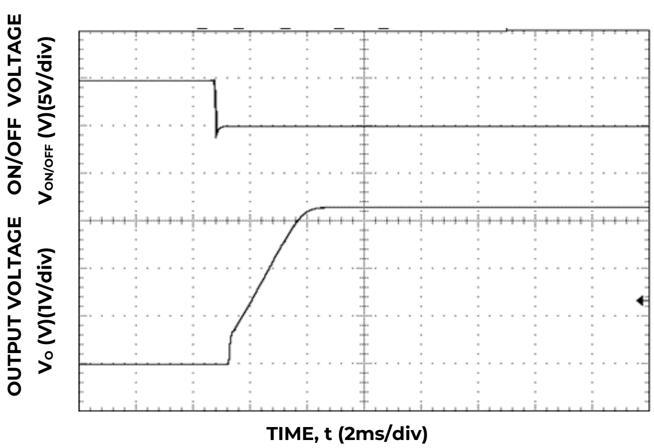


Figure 29. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

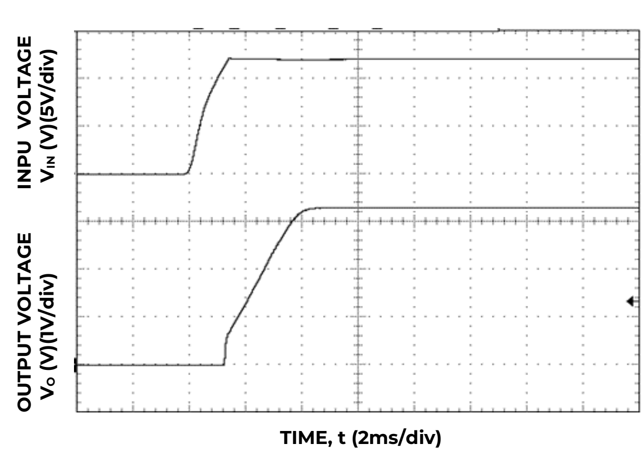


Figure 30. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o=$I_{o,max}$).

Technical Specifications (continued)

Characteristic Curves (continued)

The following figures provide typical characteristics for the 12A Analog Pico SlimLynx™ at $5V_o$ and 25°C.

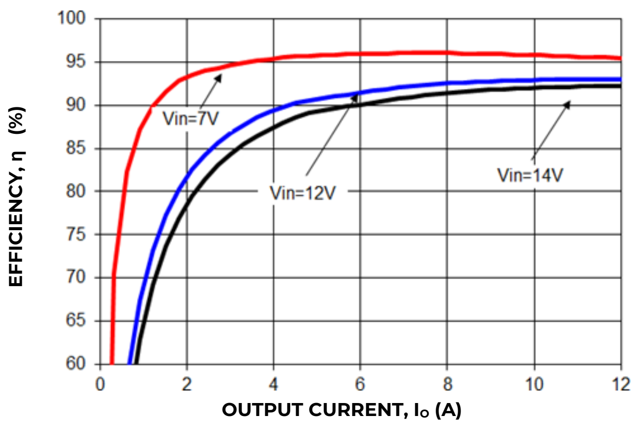


Figure 31. Converter Efficiency versus Output Current.

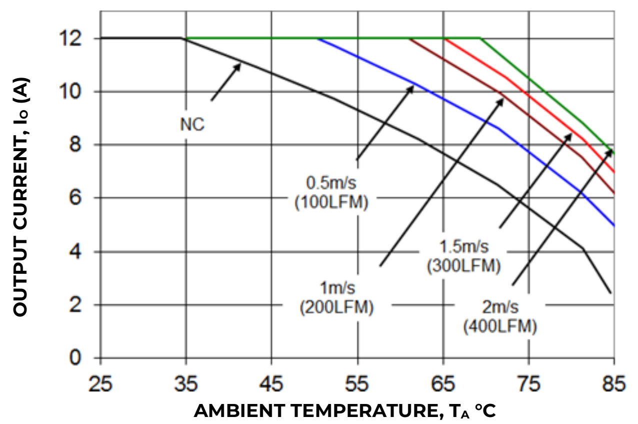


Figure 32. Derating Output Current versus Ambient Temperature and Airflow..

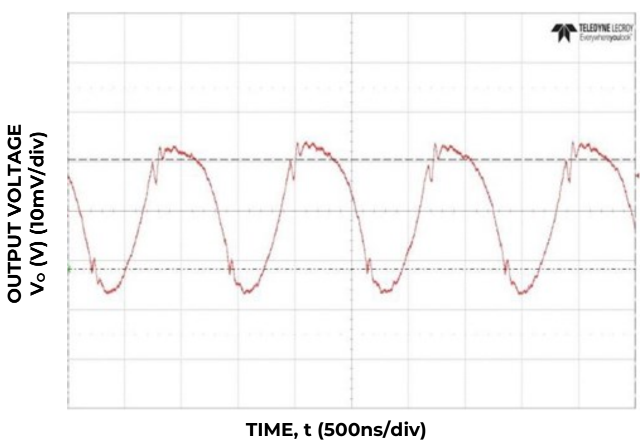


Figure 33. Typical output ripple (C_O=2x47μF ceramic, V_{IN} = 12V, I_o = $I_{o,max}$, 20MHz BW).

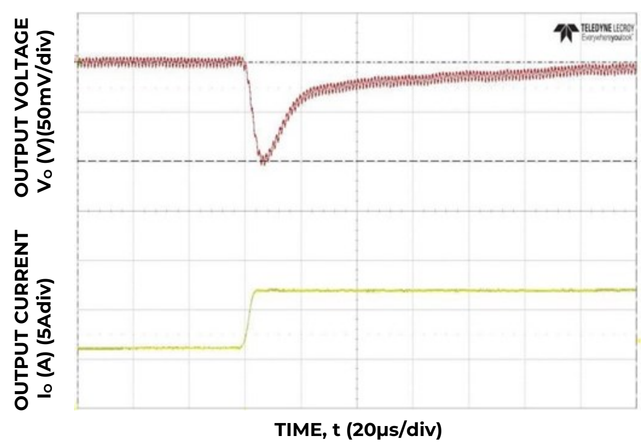


Figure 34. Transient Response to Dynamic Load Change from 50% to 100% at $12V_{in}$, C_{out}=6x47uF+1x330uF, C_{Tune}=1200pF, R_{Tune}=300

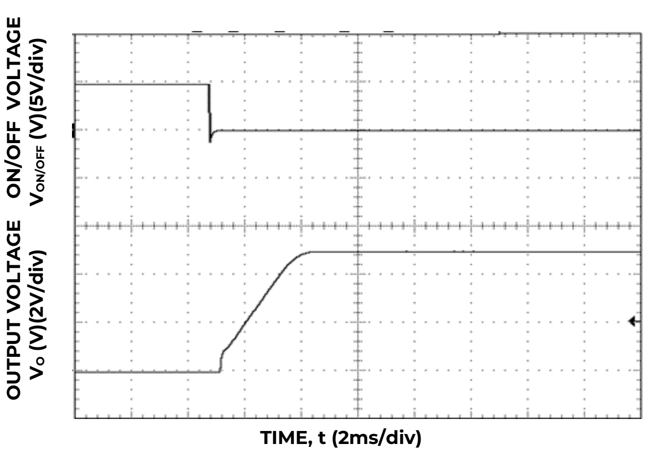


Figure 35. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

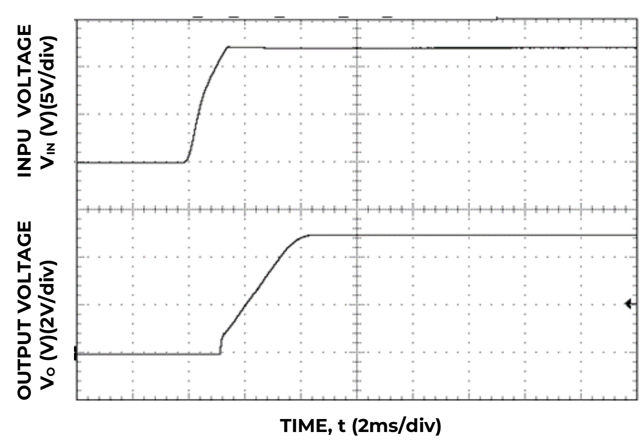


Figure 36. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o=$I_{o,max}$).

Technical Specifications (continued)

Design Considerations

Input Filtering

The 12A Analog Pico SlimLynx™ Open Frame module should be connected to a low ac-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Figure 37 shows the input ripple voltage for various output voltages at 12A of load current with 1x22 µF or 2x22 µF ceramic capacitors and an input of 12V.

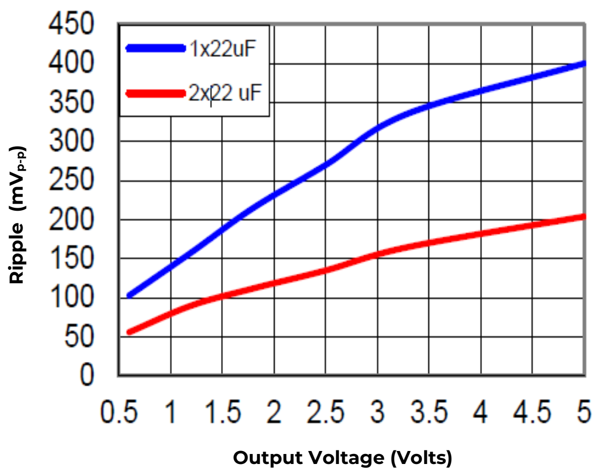


Figure 37. Input ripple voltage for various output voltages with 1x22 µF or 2x22 µF ceramic capacitors at the input (12A load). Input voltage is 12V (20MHz BW)

Output Filtering

These modules are designed for low output ripple voltage and will meet the maximum output ripple specification with 3x0.047 µF ceramic and 2x47 µF ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons. First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. Figure 38 provides output ripple information, measured with a scope with its Bandwidth limited to 20MHz for different external capacitance values at various Vo and a full load current of 12A. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table. Optimal performance of the module can be achieved by using the Tunable Loop™ feature described later in this data sheet.

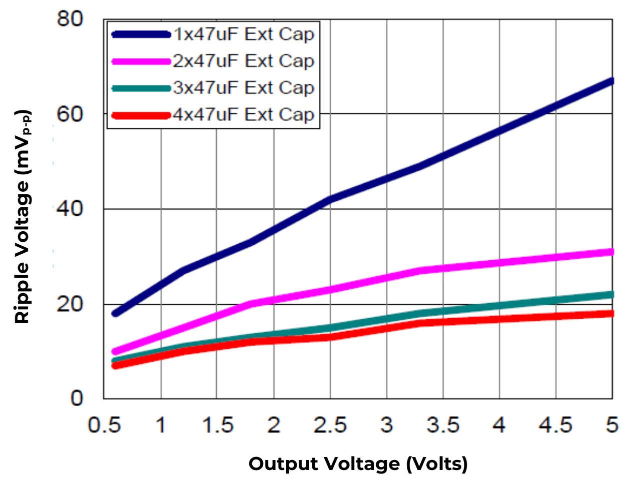


Figure 38. Output ripple voltage for various output voltages with external 2x47 µF, 4x47 µF, 6x47 µF or 8x47 µF ceramic capacitors at the output (12A load). Input voltage is 12V.(20MHz BW)

Safety Considerations

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL ANSI/UL 62368-1 and CAN/CSA C22.2 No. 62368-1 Recognized, DIN VDE 0868-1/A11:2017 (EN62368-1:2014/A11:2017)

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV) or ES1, the input must meet SELV/ES1 requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.

The input to these units is to be provided with a fast-acting fuse (e.g. ABC Bussmann) with a maximum rating of 20 A in the positive input lead.

Technical Specifications (continued)

Analog Feature Descriptions

Remote On/Off

The 12A Analog Pico SlimLynx™ Open Frame power modules feature an On/Off pin for remote On/Off operation. With the Negative Logic On/Off, (no device code suffix, see Ordering Information), the module turns OFF during logic High and ON during logic Low. The On/Off signal should be always referenced to ground. Leaving the On/Off pin disconnected will turn the module ON when input voltage is present.

For negative logic On/Off modules, the circuit configuration is shown in Fig. 39. The On/Off pin should be pulled high with an external pull-up resistor. When transistor Q1 is in the OFF state, the On/Off pin is pulled high, transistor Q2 is turned ON. This pulls the internal ENABLE low and the module is OFF. To turn the module ON, Q1 is turned ON pulling the On/Off pin low, turning transistor Q2 OFF, which results in the PWM Enable pin going high.

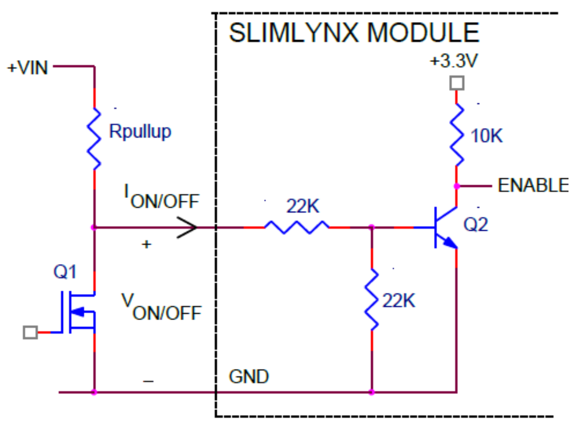


Figure 39. Circuit configuration for using positive On/Off logic.

Monotonic Start-up and Shutdown

The module has monotonic start-up and shutdown behavior for any combination of rated input voltage, output current and operating temperature range.

Startup into Pre-biased Output

The module can start into a prebiased output as long as the prebias voltage is 0.5V less than the set output voltage.

Analog Output Voltage Programming

The output voltage of the module is programmable to any voltage from 0.6dc to 5.5V_{dc} by connecting a resistor between the T_{rim} and SIG_GND pins of the module. Certain restrictions apply on the output voltage set point depending on the input voltage. These are shown in the Output Voltage vs. Input Voltage Set Point Area plot in Fig. 40. The Upper Limit curve shows that for output voltages lower than 1V, the input voltage must be lower than the maximum of 14.4V. The Lower Limit curve shows that for output voltages higher than 0.6V, the input voltage needs to be larger than the minimum of 3V.

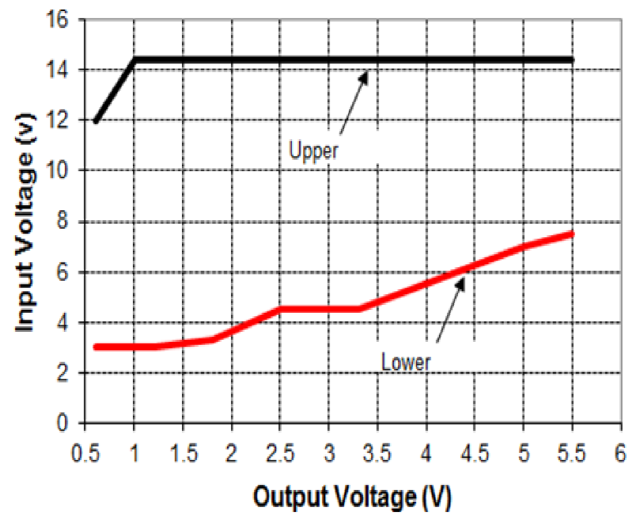


Figure 40. Output Voltage vs. Input Voltage Set Point Area plot showing limits where the output voltage can be set for different input voltages.

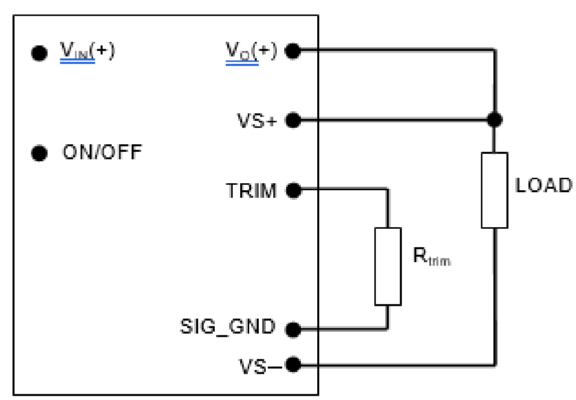


Figure 41. Circuit configuration for programming output voltage using an external resistor.

Caution – Do not connect SIG_GND to GND elsewhere in the layout

Without an external resistor between T_{rim} and SIG_GND pins, the output of the module will be 0.6V_{dc}.To calculate the value of the trim resistor, R_{trim} for a desired output voltage, should be as per the following equation:

Technical Specifications (continued)

Analog Feature Descriptions (continued)

Analog Output Voltage Programming (continued)

$$R_{trim} = \left[\frac{12}{(V_o - 0.6)} \right] K\Omega$$

R_{trim} is the external resistor in kΩ

V_o is the desired output voltage.

Table 1 provides R_{trim} values required for some common output voltages.

$V_{O,\ set}$ (V)	R_{trim} (KΩ)
0.6	Open
0.9	40
1.0	30
1.2	20
1.5	13.33
1.8	10
2.5	6.316
3.3	4.444
5.0	2.727

Table 1

Remote Sense

The power module has a Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the sense pins (VS+ and VS-). The voltage drop between the sense pins and the V_{OUT} and GND pins of the module should not exceed 0.5V.

Analog Voltage Margining

Output voltage margining can be implemented in the module by connecting a resistor, $R_{margin-up}$, from the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, $R_{margin-down}$, from the Trim pin to output pin for margining-down. Figure 42 shows the circuit configuration for output voltage margining. The POL Programming Tool, available at omnionpower.com under the Downloads section, also calculates the values of $R_{margin-up}$ and $R_{margin-down}$ for a specific output voltage and % margin. Please consult your local OmniOn Critical Power technical representative for additional details.

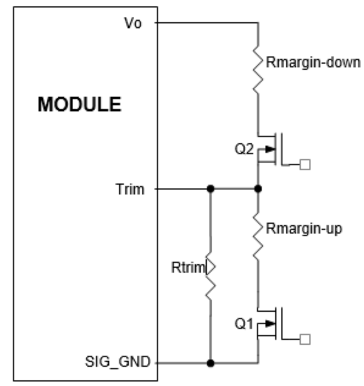


Figure 42. Circuit Configuration for margining Output voltage.

Output Voltage Sequencing

The power module includes a sequencing feature, EZ- SEQUENCE that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not using the sequencing feature, leave it unconnected.

The voltage applied to the SEQ pin should be scaled down by the same ratio as used to scale the output voltage down to the reference voltage of the module. This is accomplished by an external resistive divider connected across the sequencing voltage before it is fed to the SEQ pin as shown in Fig. 43. In addition, a small capacitor (suggested value 100pF) should be connected across the lower resistor R1.

For all SlimLynx modules, the minimum recommended delay between the ON/OFF signal and the sequencing signal is 10ms to ensure that the module output is ramped up according to the sequencing signal. This ensures that the module soft-start routine is completed before the sequencing signal is allowed to ramp up.

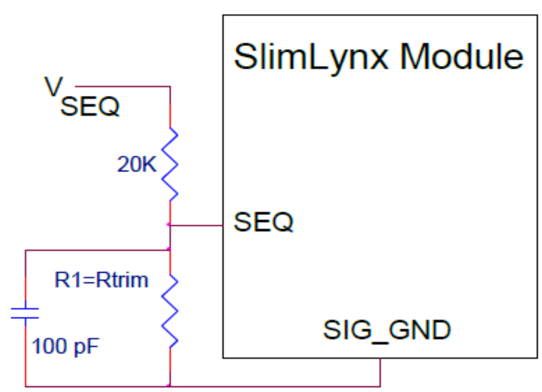


Figure 43. Circuit showing connection of the sequencing signal to the SEQ pin.

Technical Specifications (continued)

Analog Feature Descriptions (continued)

Output Voltage Sequencing (continued)

When the scaled down sequencing voltage is applied to the SEQ pin, the output voltage tracks this voltage until the output reaches the set-point voltage. The final value of the sequencing voltage must be set higher than the set-point voltage of the module. The output voltage follows the sequencing voltage on a one-to-one basis. By connecting multiple modules together, multiple modules can track their output voltages to the voltage applied on the SEQ pin.

The module's output can track the SEQ pin signal with slopes of up to 0.5V/msec during power-up or power-down.

To initiate simultaneous shutdown of the modules, the SEQ pin voltage is lowered in a controlled manner. The output voltage of the modules tracks the voltages below their set-point voltages on a one-to-one basis. A valid input voltage must be maintained until the tracking and output voltages reach ground potential

Overcurrent Protection

To provide protection in a fault (output overload) condition, the unit is equipped with internal current-limiting circuitry and can endure current limiting continuously. At the point of current-limit inception, the unit enters hiccup mode. The unit operates normally once the output current is brought back into its specified range.

Overtemperature Protection

To provide protection in a fault condition, the unit is equipped with a thermal shutdown circuit. The unit will shut down if the overtemperature threshold of 150oC(typ) is exceeded at the thermal reference point Tref .Once the unit goes into thermal shutdown it will then wait to cool before attempting to restart.

Input Undervoltage Lockout

At input voltages below the input undervoltage lockout limit, the module operation is disabled. The module will begin to operate at an input voltage above the undervoltage lockout turn-on threshold.

Synchronization

The module switching frequency can be synchronized to a signal with an external frequency within a specified range. Synchronization can be done by using the external signal applied to the SYNC pin of the module as shown in Fig. 44, with the converter being synchronized by the rising edge of the external signal. The Electrical Specifications table specifies the requirements of the external SYNC signal. If the SYNC pin is not used, the module should free run at the default switching frequency. If synchronization is not being used, connect the SYNC pin to GND.

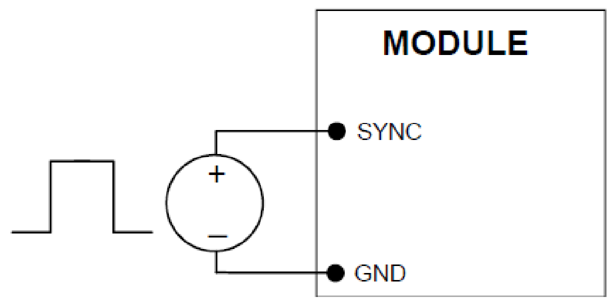


Figure 44. External source connections to synchronize switching frequency of the module.

Tunable Loop™

The module has a feature that optimizes transient response of the module called Tunable Loop™.

External capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise (see Figure 38) and to reduce output voltage deviations from the steady-state value in the presence of dynamic load current changes. Adding external capacitance however affects the voltage control loop of the module, typically causing the loop to slow down with sluggish response. Larger values of external capacitance could also cause the module to become unstable.

The Tunable Loop™ allows the user to externally adjust the voltage control loop to match the filter network connected to the output of the module. The Tunable Loop™ is implemented by connecting a series R-C between the VS+ and TRIM pins of the module, as shown in Fig. 45. This R-C allows the user to externally adjust the voltage loop feedback compensation of the module.

Technical Specifications (continued)

Analog Feature Descriptions (continued)

Tunable Loop™ (continued)

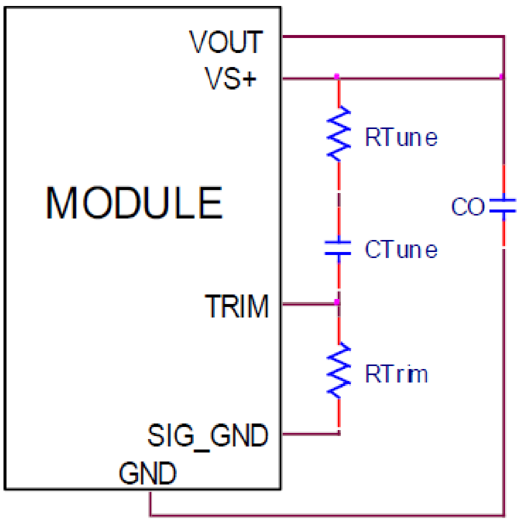


Figure. 45. Circuit diagram showing connection of R_{TUME} and C_{TUNE} to tune the control loop of the module.

Recommended values of R_{TUNE} and C_{TUNE} for different output capacitor combinations are given in Table 2. Table 2 shows the recommended values of R_{TUNE} and C_{TUNE} for different values of ceramic output capacitors up to 1000uF that might be needed for an application to meet output ripple and noise requirements. Selecting R_{TUNE} and C_{TUNE} according to Table 2 will ensure stable operation of the module.

In applications with tight output voltage limits in the presence of dynamic current loading, additional output capacitance will be required. Table 3 lists recommended values of R_{TUNE} and C_{TUNE} in order to meet 2% output voltage deviation limits for some common output voltages in the presence of a 6A to 12A step change (50% of full load), with an input voltage of 12V. Please contact your OmniOn Critical Power technical representative to obtain more details of this feature as well as for guidelines on how to select the right value of external R-C to tune the module for best transient performance and stable operation for other output capacitance values.

C_o	3x47μF	4x47μF	6x47μF	10x47μF	20x47μF
R_{TUNE}	300	300	300	300	300
C_{TUNE}	680p	820p	1200p	2700pF	5600pF

Table 2. General recommended values of of R_{TUNE} and C_{TUNE} for V_{in}=12V and various external ceramic capacitor combinations.

V_o	5V	3.3V	2.5V	1.8V	1.2V	0.6V
C_o	6x47uf Ceramic	4x47uF+ 1x330uF Polymer	4x47uF+ 1x330uF Polymer	4x47uF+ 2x330uF Polymer	4x47uF+ 3x330uF Polymer	3x47uF+ 4x330uF Polymer
R_{TUNE}	300	300	300	300	300	300
C_{TUNE}	1200pF	1800pF	2700pF	8200pF	10nF	47nF
ΔV	89mV	62mV	49mV	33mV	24mV	11mV

Table 3. Recommended values of R_{TUNE} and C_{TUNE} to obtain transient deviation of 2% of V_{out} for a 6A step load with V_{in}=12V.

Note: The capacitors used in the Tunable Loop tables are 47 μF/2 mΩ ESR ceramic and 330 μF/9 mΩ ESR polymer capacitors.

Power Good

The module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as over temperature, overcurrent or loss of regulation occurs that would result in the output voltage going outside the specified thresholds.

The PGOOD terminal can be connected through a pullup resistor (suggested value 100KΩ) to a source of $5V_{DC}$ or lower.

Technical Specifications (continued)

Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation.

Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Figure 46. The preferred airflow direction for the module is in Figure 47.

The thermal reference points, T_{ref} used in the specifications are also shown in Figure 47. For reliable operation the temperatures at the Q3 should not exceed 120°C and the temperature at L1 core should not exceed 125°C. The output power of the module should not exceed the rated power of the module ($V_{o,set}$ x $I_{o,max}$).

Please refer to the Application Note "Thermal Characterization Process For Open-Frame Board Mounted Power Modules" for a detailed discussion of thermal aspects including maximum device temperatures.

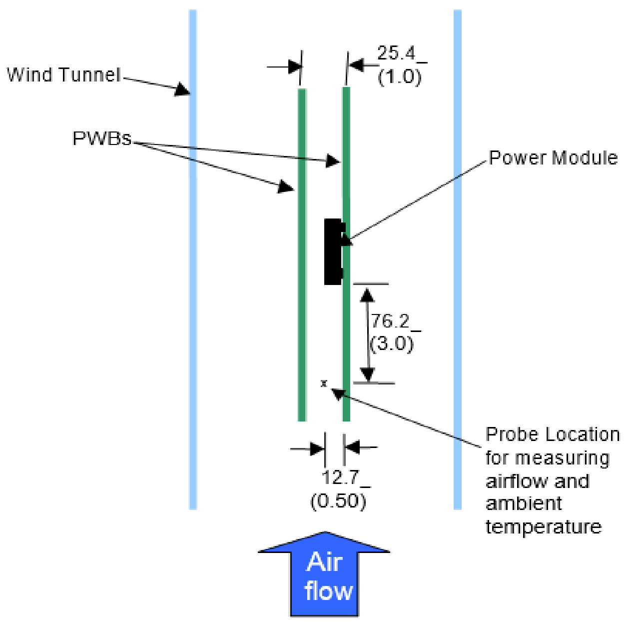


Figure 46. Thermal Test Setup.

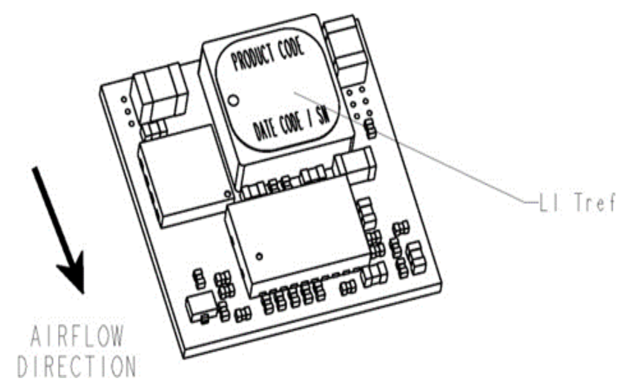


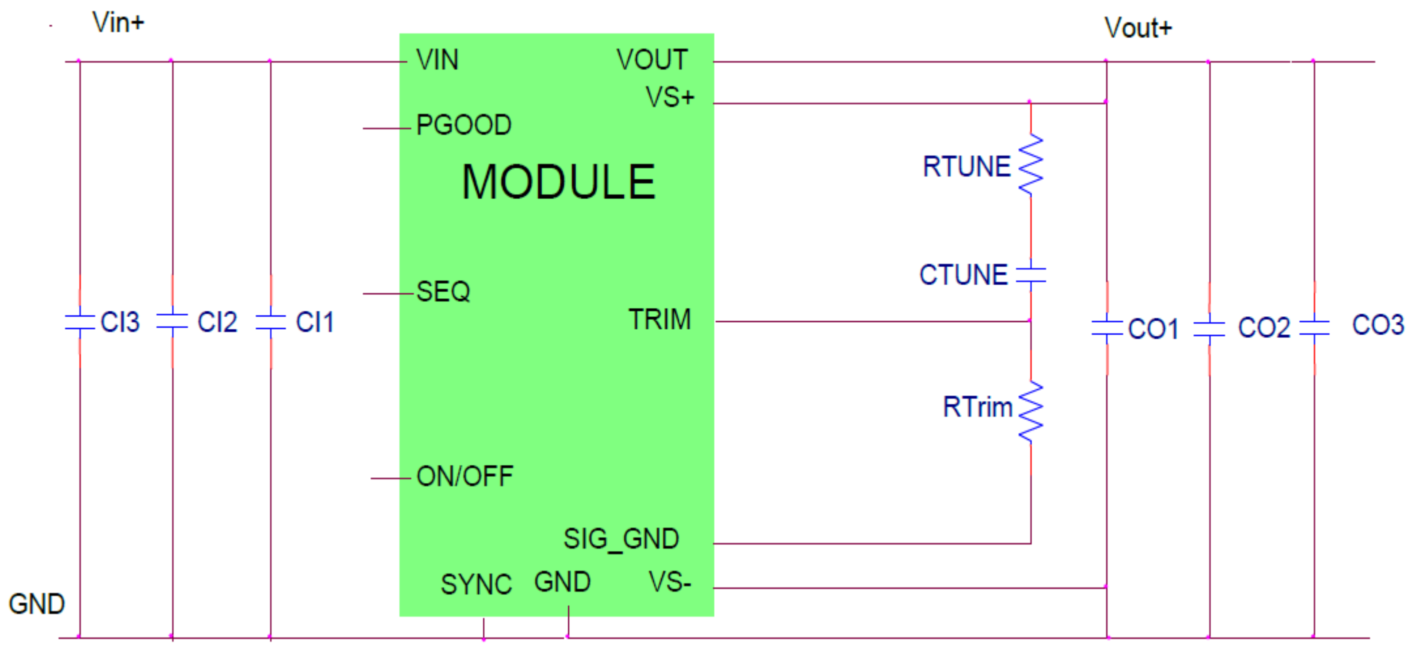
Figure 47. Preferred airflow direction and location of hot- spot of the module (T_{ref}).

Technical Specifications (continued)

Example Application Circuit

Requirements:

V_{in}:	12V
V_{out}:	1.8V
I_{out}:	9A max., worst case load transient is from 6A to 9A
DV_{out}:	1.5% of V_{out} (27mV) for worst case load transient
$V_{in,\ ripple}$	1.5% of V_{in} (180mV, p-p)



CI1	Decoupling cap - 1x0.047μF/16V ceramic capacitor (e.g. Murata LLL185R71C473MA01)
CI2	2x22μF/16V ceramic capacitor (e.g. Murata GRM32ER61C226KE20)
CI3	470μF/16V bulk electrolytic
CO1	Decoupling cap - 1x0.047μF/16V ceramic capacitor (e.g. Murata LLL185R71C473MA01) + 1x0.047uF/16V 0402 size ceramic capacitor
CO2	3x47μF/16V ceramic capacitor (e.g. Murata GRM32ER61C226KE20)
CO3	1x330μF/6V POSCAP
C_{Tune}	3900pF ceramic capacitor (can be 1206, 0805 or 0603 size)
R_{Tune}	300 ΩSMT resistor (can be 1206, 0805 or 0603 size)
R_{Trim}	10kμ SMT resistor (can be 1206, 0805 or 0603 size, recommended tolerance of 0.1%)

Note: The DATA, CLK and SMBALRT pins do not have any pull-up resistors inside the module. Typically, the SMBus master controller will have the pull-up resistors as well as provide the driving source for these signals.

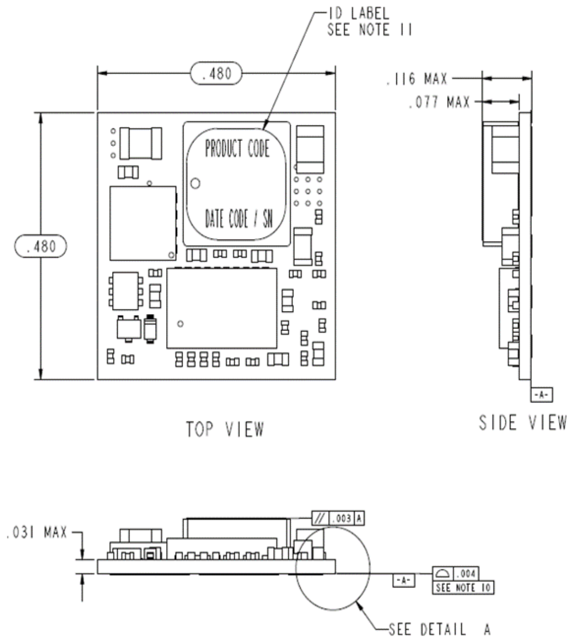
Technical Specifications (continued)

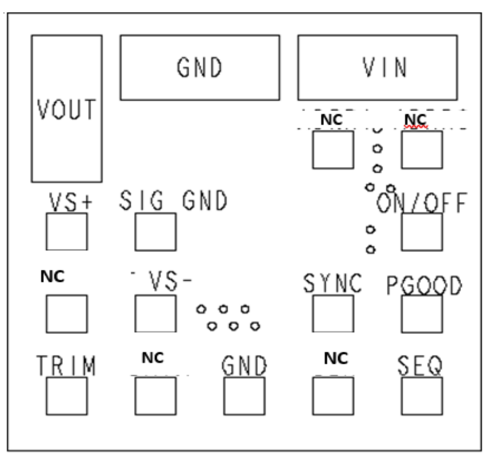
Mechanical Outline

Dimensions are in millimeters and (inches).

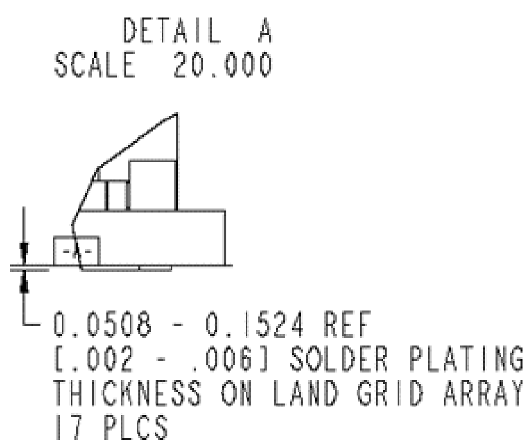
Tolerances: x.x mm ±0.5 mm (x.xx in. ± 0.02 in.) [unless otherwise indicated]

x.xx mm ± 0.25 mm (x.xxx in ± 0.010 in.)





BOTTOM VIEW



PIN	FUNCTION	PIN	FUNCTION
1	ON/OFF	10	PGOOD
2	V_{IN}	11	SYNC[2]
3	GND	12	VS-
4	V_{OUT}	13	SIG_GND
5	VS+ (SENSE)	14	NC
6	TRIM	15	NC
7	GND	16	NC
8	NC	17	NC
9	SEQ		

[2] If unused, connect Ground

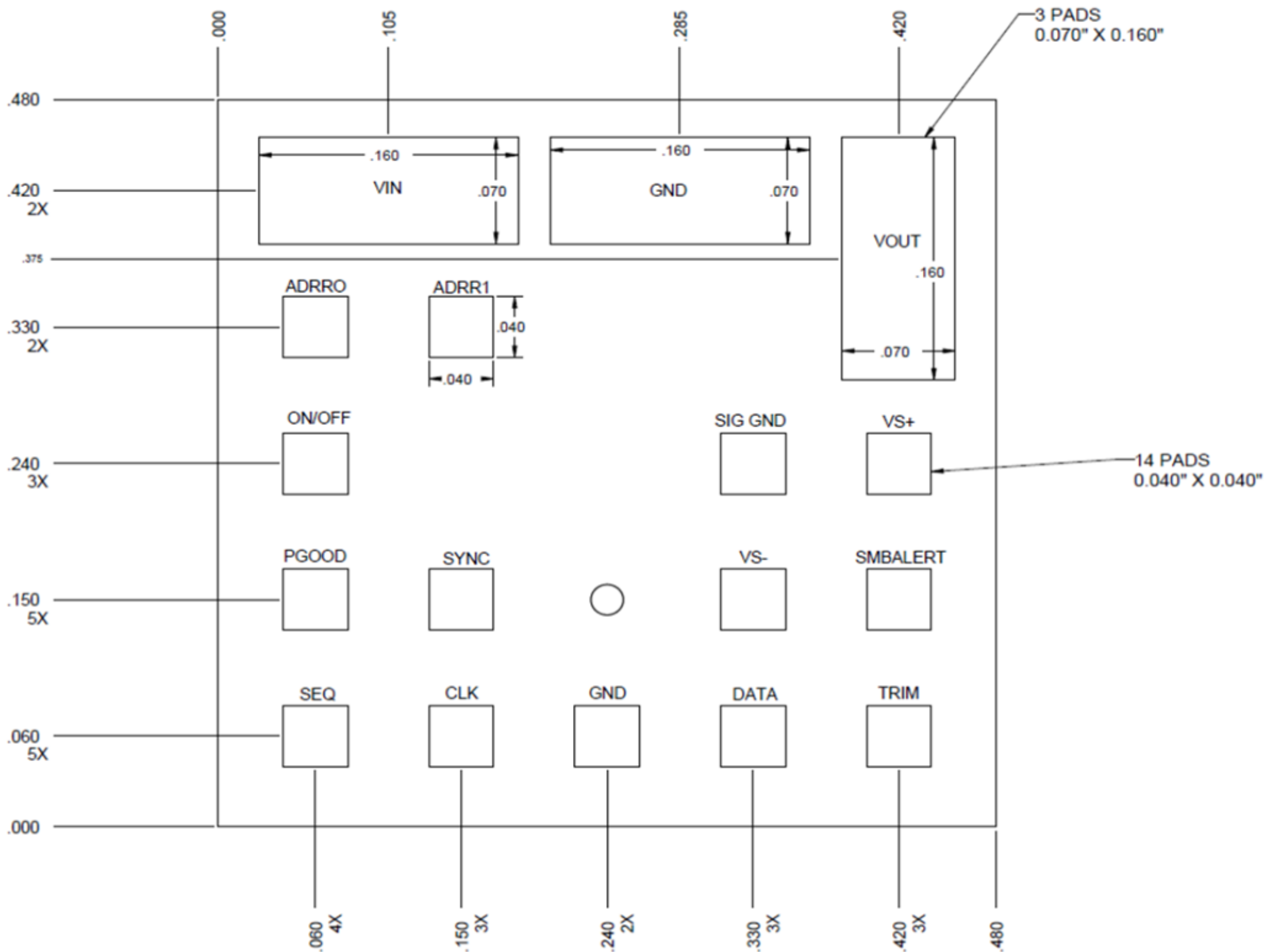
Technical Specifications (continued)

Recommended Pad Layout

Dimensions are in millimeters and (inches).

Tolerances: x.x mm ±0.5 mm (x.xx in. ± 0.02 in.) [unless otherwise indicated]

x.xx mm ± 0.25 mm (x.xxx in ± 0.010 in.)



PIN	FUNCTION	PIN	FUNCTION
1	ON/OFF	10	PGOOD
2	V_{IN}	11	SYNC[2]
3	GND	12	VS-
4	V_{OUT}	13	SIG_GND
5	VS+ (SENSE)	14	NC
6	TRIM	15	NC
7	GND	16	NC
8	NC	17	NC
9	SEQ		

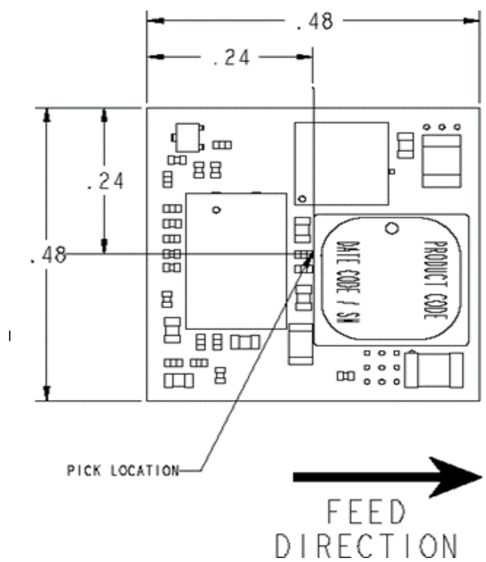
[2]If unused, connect to Ground.

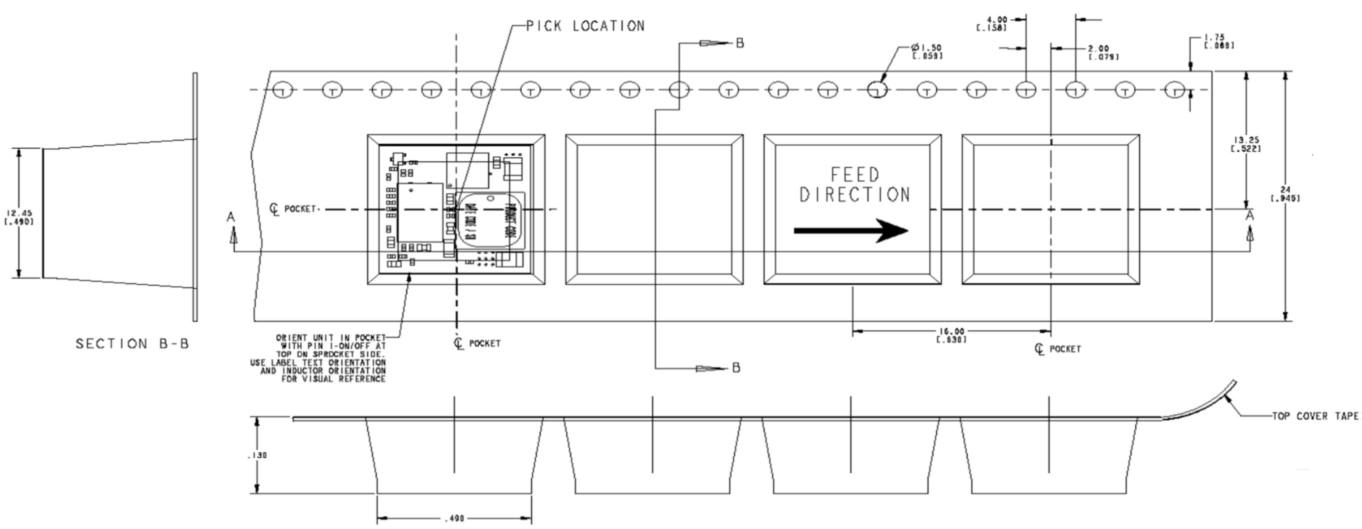
Technical Specifications (continued)

Packaging Details

The 12V Analog Pico SlimLynx™ 12A Open Frame modules are supplied in tape & reel as standard. Modules are shipped in quantities of 500 modules per reel.

All Dimensions are in millimeters and (in inches).





Reel Dimensions:

Outside Dimensions:	254 mm (13.00)
Inside Dimensions:	177.8 mm (7.00”)
Tape Width:	24.00 mm (0.945”)

Technical Specifications (continued)

Surface Mount Information

Pick and Place

The 12A Analog Pico SlimLynx™ Open Frame modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300°C. The label also carries product information such as product code, serial number and the location of manufacture.

Nozzle Recommendations

The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7 mm.

Lead Free Soldering

The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

Pb-free Reflow Profile

Power Systems will comply with J-STD-020 Rev. D (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended linear reflow profile using Sn/Ag/Cu solder is shown in Fig. 48. Soldering outside of the recommended profile requires testing to verify results and performance.

MSL Rating

The 12A Analog Pico SlimLynx™ Open Frame modules have a MSL rating of 2a.

Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture/ Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of ≤ 30°C and 60% relative humidity varies according to the MSL rating (see J- STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40°C, < 90% relative humidity.

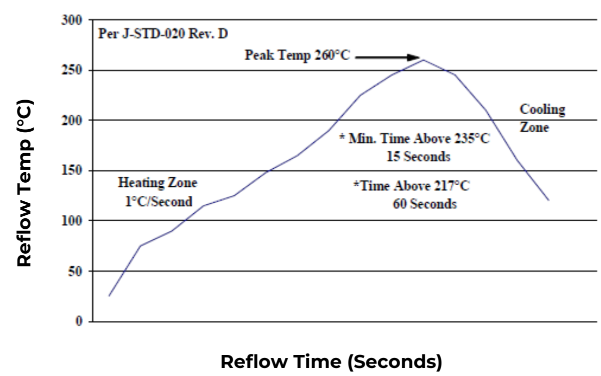


Figure 48. Recommended linear reflow profile using Sn/Ag/Cu solder.

Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to Board Mounted Power Modules: Soldering and Cleaning Application Note (AN04-001).

Ordering Information

Please contact your OmniOn Sales Representative for pricing, availability and optional features.

Device Code	Input Voltage Range	Output Voltage	Output Current	On/Off Logic	Sequencing	Ordering Code
PNVT012A0X3-SRZ	3 – 14.4V_{dc}	0.6 – 5.5V_{dc}	12A	Negative	Yes	150038561

Table 4. Device Codes

-Z refers to RoHS compliant parts

Package Identifier	Family	Sequencing Option	Output current	Output voltage	On/Off logic	Remote Sense	Options	RoHS Compliance
P	**NV**	**T**	**012A0**	**X**		**3**	**-SR**	**Z**
P=Pico U=Pico M=Mega G=Giga	NV=SlimLynx Analog Open Frame	T=with EZ Sequence X = without sequencing	12A	X = programmable output	No entry = negative	3 = Remote Sense	S = Surface Mount R = Tape & Reel	Z = RoHS6

Table 5 . Coding Scheme

Contact Us

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Change History (excludes grammar & clarifications)

Revision	Date	Description of the change
7.3	15/11/2021	Updated as per template
7.4	12/13/2023	Updated as per OmniOn template

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