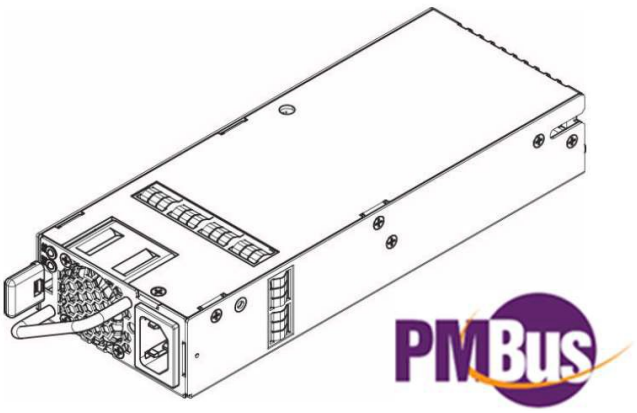
# MPR0854FP series front-end

## Input: 100-120/200-240$V_{AC}$; Output: 54$V_{DC}$ @ 800W; 12$V_{DC}$ @ 0.8A

RoHS Compliant




## Description

The MPR0854FP series of front ends provide efficient isolated power from world-wide commercial AC mains. Offered in the industry standard compact 1U form factor, these front ends provide comprehensive solutions for systems connected to commercial ac mains.

This high-density front end can be ordered either as a front-to-back or back-to-front airflow product. It is designed for minimal space utilization and is highly expandable for future growth. The industry standard PMBus compliant $I^2C$ communications buss offers a full range of control and monitoring capabilities. on cost and PWB area.

## Applications

- 48$V_{DC}$ distributed power architectures
- Datacom and Telecom applications
- Mid to high-end Servers
- Enterprise Networking
- Network Attached Storage
- Telecom Access Nodes
- Routers/Switches
- ATE Equipment

## Features

- Output voltage set to 54$V_{dc}$
- Universal input with PFC
- No power de-rating at low line input range
- 2 front panel LEDs: LED1 - input
  LED2 - [output, fault, over temp]
- Remote ON/OFF control of the 54$V_{DC}$ output
- Remote sense on the 54$V_{DC}$ output
- Meets Power-Over-Ethernet (IEEE802.3af)
- No minimum load requirements
- Droop load sharing
- Hot Plug-able
- Efficiency: typically 92.5% @ 50% load and 90.0% @ 20% load
- 12$V_{DC}$ for backup power
- Auto recoverable OC & OT protection
- Radiated emissions hardened enclosure
- Operating temperature: -10 - 70°C (de-rated above 50°C)
- Digital status & control: PMBus™ compliant serial bus
- EN/IEC/UL62368-1 2nd edition; UL, CSA and VDE
- EMI: class A FCC docket 20780 part 15, EN55032
- Meets EN6100 immunity and transient standards
- Shock & vibration: IEC-68-2
- Compliant to RoHS Directive 2011/65/EU and amended Directive (EU) 2015/863.

FOOTNOTES:
* UL is a registered trademark of Underwriters Laboratories, Inc.
† CSA is a registered trademark of Canadian Standards Association.
‡ VDE is a trademark of Verband Deutscher Elektrotechniker e.V.
§ Intended for integration into end-user equipment. All the required procedures for CE marking of end-user equipment should be followed. (The CE mark is placed on selected products.)
** ISO is a registered trademark of the International Organization of Standards.
+ PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF)

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage: Continuous | $V_{IN}$ | 0 | 264 | VAC |
| Operating Ambient Temperature | $T_A$ | -10 | 70[1] | °C |
| Storage Temperature | $T_{stg}$ | -40 | 85 | °C |
| I/O Isolation voltage to Frame (100% factory Hi-Pot tested) | | | 1500 | $V_{AC}$ |

[1] Derated above 50°C at 2.5%/°C

## Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions.

**INPUT**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operational Range | | $V_{IN}$ | 90 | 110/230 | 264 | $V_{AC}$ |
| Frequency Range | | FIN | 47 | 50/60 | 63 | Hz |
| Main Output Turn_OFF | | $V_{IN}$ | 68 | | 75 | $V_{AC}$ |
| Main Output Turn ON | | $V_{IN}$ | 76 | | 84 | $V_{AC}$ |
| Maximum Input Current ($V_{OUT}$= 54$V_{DC}$, $I_{OUT}$=14.8A) | $V_{IN}$= 100$V_{AC}$ | $I_{IN}$ | | | 9.2 | $A_{AC}$ |
| | $V_{IN}$= 200$V_{AC}$ | | | | 4.6 | |
| Cold Start Inrush Current (Excluding x-caps, 25°C) | | $I_{IN}$ | | | 30 | $A_{PEAK}$ |
| | duration | | | | ½ | cycle |
| Efficiency ($T_{AMB}$=25°C, $V_{OUT}$ = 54$V_{DC}$, $I_O$ = 14.8A) | input | | 100-240 | | | $V_{IN}$ |
| | 100% load | η | 88 | | | % |
| | 75% load | | 87 | | | |
| | 50% load | | 84 | | | |
| | 20% load | | 77 | | | |
| Power Factor (Vin=90 - 264$V_{AC}$, $I_{OUT}$ = 14.8A) | | PF | 0.8 | 0.99 | | |
| Holdup time ($V_{IN}$ = 90$V_{AC}$, $T_{AMB}$ 25°C, $V_{OUT}$ = 54$V_{DC}$, IOUT = 14.8A) | | T | 10 | | | ms |
| Power Fail Warning (AC_OK_L) | Assertion delay[2] | T | 10 | | | ms |
| | Start of assetion[3] | | 5 | | | ms |
| | Level of voltage decay | $V_{DC}$ | 43 | | | $V_{DC}$ |
| Leakage Current ($V_{IN}$= 264$V_{AC}$, $F_{IN}$ = 60Hz) | | $I_{IN}$ | | | 3.5 | mA |
| Isolation | Input/Output | $V_{AC}$ | 3000 | | | $V_{AC}$ |
| | Input/Frame | | 1500 | | | $V_{AC}$ |
| | Main output or main_rtn/Frame | $V_{DC}$ | 2121 | | | $V_{DC}$ |
| | 3.3$V_{STNDBY}$ or 12V /main output | | 2121 | | | $V_{DC}$ |

[2] PFW does not trigger for power interruptions lasting less than 10ms (½ cycle)

[3] The signal shall assert at least 5ms prior to decaying of the output voltage below 43VDC

## Electrical Specifications (continued)

**54$V_{DC}$ MAIN OUTPUT**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Power | | W | 0 | - | 800 | W |
| Regulation | Set point ($V_{IN}$ = 100$V_{AC}$, $T_{AMB}$ 25°C, $I_{OUT}$ = 7.4A) | $V_{OUT}$ | 53.95 | 54.00 | 54.05 | $V_{DC}$ |
| | Temperature drift | | | | 0.01 | %/°C |
| | Overall regulation (line, load, temperature) | | -5 | | +5 | % |
| | Maximum remote sense voltage | | | | 0.5 | $V_{DC}$ |
| Ripple and noise[4] (meets IEEE802.3af for POE) | f < 500Hz | $V_{OUT}$ | | | 600 | $mV_{p-p}$ |
| | f = 500 – 150kHz | | | | 200 | |
| | f = 150kHz – 500kHz | | | | 150 | |
| | f = 500kHz – 1MHz | | | | 100 | |
| Turn-ON or turn-OFF overshoot | | | | | +0 | % |
| Turn-ON delay to within regulation | | T | | | 3 | sec |
| Remote ON/OFF delay time | | | | 40 | | ms |
| Turn-ON monotonic rise time (10 – 90% of $V_{OUT}$) | | | | 150 | | ms |
| Transient response 25% step [10%-35%, 100% - 75%] (di/dt – 1A/µs, recovery to within 2% of nominal in 500µs) | | $V_{OUT}$ | -5 | | +5 | $\%V_{OUT}$ |
| Overvoltage protection, latched (recovery by cycling OFF/ON via hardware or software) | | | 57.5 | | 60 | $V_{DC}$ |
| Output current | | $I_{OUT}$ | 0 | | 14.8 | $V_{DC}$ |
| Current limit, Foldback | | | 16 | | 20 | $A_{DC}$ |
| Droop current share (linear from no-load to full-load) | Output voltage at 0 load | | | 55.62 | | $V_{DC}$ |
| | Output voltage at 14,8A load | | | 52.38 | | |
| | Permissible load difference between power supplies | | | | 3 | $A_{DC}$ |

[4] Measured across a 10µf electrolytic and a 0.1µf ceramic capacitors in parallel. 20MHz bandwidth

**12$V_{DC}$ Back-bias OUTPUT**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Set point | $V_{OUT}$ | | 12 | | $V_{DC}$ |
| Overall regulation (load, temperature, aging) with | $V_{OUT}$ | 8.5 | | 13 | V |
| Ripple and noise | | | 0.29 | 0.65 | $V_{rms}$ |
| Output current | $I_{OUT}$ | 0 | | 0.5 | $A_{DC}$ |
| IsolationOutput/Frame | | 100 | | | $V_{DC}$ |

## General Specifications

| Parameter | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|
| Reliability | | 300,000<br>100,000 | | hrs | Full load, 25°C per Bellcore RPP<br>Full load, 50°C per Bellcore RPP |
| Service Life | | 10 | | Yrs | Full load, excluding fans |
| Weight | | 1.09 (2.4) | 1.4(3.1) | Kgs (Lbs) | |

## Feature Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. All signals are referenced to Signal_Return unless otherwise noted. See Feature Descriptions for additional information. ( $I_{OL}$ < 5mA, $I_{OH}$ < 20µA )

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| MODULE_ENABLE_L [short pin controlling presence of the 54V output] | | | | | |
| 54V output OFF | $V_I$ | 0.7 $V_{DD}$ | — | 5 | $V_{DC}$ |
| 54V output ON | $V_I$ | 0 | — | 0.8 | $V_{DC}$ |
| AC_OK_L [PFW] (Needs to be pulled HI via an external resistor) | | | | | |
| Logic HI (Input out-of-normal range) | $V_{OH}$ | 0.7 $V_{DD}$ | — | 5 | $V_{DC}$ |
| Logic LO (Input within normal range) | $V_{OL}$ | 0 | | 0.4 | $V_{DC}$ |
| DC_OK_L (Needs to be pulled HI via an external resistor) | | | | | |
| Logic HI — Output voltage is not within limits | $V_{OH}$ | 0.7$V_{DD}$ | — | 5 | $V_{DC}$ |
| Level shift for out of limits ( $V_{OUT}$ transitioning low) | | 47 | | 51 | $V_{DC}$ |
| Logic LO — Output voltage is within limits | $V_{OL}$ | 0 | — | 0.4 | $V_{DC}$ |
| Level shift for within limits ($V_{OUT}$ transitioning high) | | 51 | | 52 | $V_{DC}$ |
| TEMP_OK_L (Needs to be pulled HI via an external resistor) | | | | | |
| Logic HI (temperature is too high) | $V_{OH}$ | 0.7$V_{DD}$ | — | 5 | $V_{DC}$ |
| Logic LO (temperature within normal range) | $V_{OL}$ | 0 | — | 0.4 | $V_{DC}$ |
| Delayed shutdown after Logic HI transition | $T_{delay}$ | 150 | | | ms |
| PS_Present_L (Needs to be pulled HI via an external resistor) | | | | | |
| Logic LO | $V_{IL}$ | 0 | — | 0.1 | $V_{DC}$ |
| Module_Enable_L | | | | | |
| Logic LO (normally connected to Signal_Return in the system) | $V_{IL}$ | 0 | — | 0.1 | $V_{DC}$ |
| $I^2C$ address signals A0, A1, A2 (internally pulled HI) | | | | | |
| Logic LO | $V_{IL}$ | 0 | — | 0.1 | $V_{DC}$ |
| $I^2C$ Clock and Data Lines (internally pulled up to 3.3VDC via 1.2kΩ) | | | | | |
| Logic HI | $V_{OH}$ | 0.7$V_{DD}$ | — | 3.3 | $V_{DC}$ |
| Logic LO (Data line sync by the power supply) | $V_{OL}$ | 0 | — | 0.4 | $V_{DC}$ |
| Logic LO (interpreted by the power supply) | $V_{OL}$ | 0 | — | 0.8 | $V_{DC}$ |

## Digital Interface Specification

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PMBus Signal Interface Characteristics | | | | | | |
| Input Logic High Voltage (CLK, DATA) | | $V_{IH}$ | 2.1 | | 3.6 | $V_{DC}$ |
| Input Logic Low Voltage (CLK, DATA) | | $V_{IL}$ | 0 | | 0.8 | $V_{DC}$ |
| Input high sourced current (CLK, DATA) | | $I_{IH}$ | 0 | | 10 | µA |
| Output Low sink Voltage (CLK, DATA) | $I_{OUT}$=3.5mA | $V_{OL}$ | | | 0.4 | $V_{DC}$ |
| Output Low sink current (CLK, DATA) | | $I_{OL}$ | 3.5 | | | mA |
| Output High open drain leakage current (CLK,DATA) | $V_{OUT}$=3.6V | $I_{OH}$ | 0 | | 10 | µA |
| PMBus Operating frequency range | Slave Mode | $F_{PMB}$ | 10 | | 400 | kHz |
| Measurement System Characteristics (all measurement tolerances are typical estimations under normal operating conditions) | | | | | | |
| Clock stretching | | $t_{STRETCH}$ | | | 25 | ms |
| $I_{OUT}$ measurement range | Linear | $I_{RNG}$ | 0 | | 25 | $A_{DC}$ |
| $I_{OUT}$ measurement accuracy 25°C | | $I_{ACC}$ | -3 | | +3 | % |
| $V_{OUT}$ measurement range | Linear | $V_{OUT(rng)}$ | 0 | | 75 | $V_{DC}$ |
| $V_{OUT}$ measurement accuracy | | $V_{OUT(acc)}$ | -2 | | +2 | % |
| $T_{emp}$ measurement range | Linear | $T_{emp(rng)}$ | 0 | | 120 | °C |
| Temp measurement accuracy[5] | | $Temp_{(acc)}$ | -5 | | +5 | % |
| Fan Speed measurement range | Linear | | 0 | | 30k | RPM |
| Fan Speed measurement accuracy | | | -2 | | 2 | % |

[5] Temperature accuracy reduces non-linearly with decreasing temperature

## Environmental Specifications

| Parameter | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|
| Ambient Temperature | 0 | | 50 | °C | |
| Storage Temperature | -40 | | 85 | °C | |
| Operating Altitude | | | 1524/5000 | m/ft | |
| Non-operating Altitude | | | 15240/50k | m / ft | |
| Power Derating with Altitude | | | 2.0 | C°/301 m<br>C°/1000 ft | |
| Acoustic noise | | | 55 | dbA | 25°C and Full load |
| OT (TEMP_OK_L) Warning<br>Protection<br>Recovery hysteresis | 150 | <br>110[6]<br>5 | | ms<br>°C<br>°C | Prior to shutdown<br>Default: Auto-recoverable |
| Humidity<br>Operating<br>Storage | <br>5<br>5 | | <br>95<br>95 | % | Relative humidity, non-condensing |
| Vibration | | | 0.2 | G | IEC 68-2-6, 5-500Hz |
| Shock | | | 10 | G | IEC 68-2-27, 10ms intervals 3 shocks |

[6] Designed such that device junction thresholds do not exceed 110°C under normal operating conditions

## EMC Compliance

| Parameter | Criteria | Standard | Level | Test |
|---|---|---|---|---|
| AC input | Conducted emissions | FCC and CISPR (EN55032A, VCCI-2) | A +6dB | 0.15 – 30MHz |
| Radiated emissions | | EN55032 | A +6dB | 30 – 10000MHz |
| Harmonic current | Emissions | EN-61000-3-2 | Table 1 | |
| Voltage | Fluctuations & Flicker | En-61000-3-3 | | |
| AC Input immunity | Voltage dips | EN61000-4-11 | A | -30%, 10ms |
| | | | B | -60%, 100ms |
| | | | B | -100%, 5sec |
| | Voltage surge | EN61000-4-5 | A | 2kV, 1.2/50µs, common mode |
| | | | A | 1kV, 1.2/50µs, differential mode |
| | Fast transients | EN61000-4-4 | B | ±0.5kV on data lines, ±1kV on power lines, 5kHz rate |
| Enclosure immunity | Conducted RF fields | EN61000-4-6 | A | 130dBµV, 0.15-80MHz, 80% AM |
| | Radiated RF fields | EN61000-4-3 | A | 3V/m, 80-1000MHz, 80% AM |
| | | ENV 50140 | A | |
| | ESD | EN61000-4-2 | B | ±4kV contact, ±8kV air |

## Characteristic Curves

The following figures provide typical characteristics at 25°C

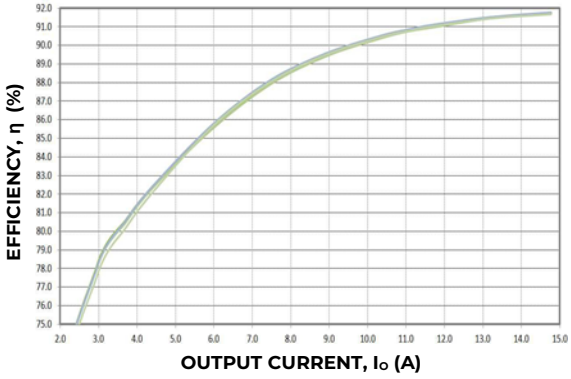



**Figure 1. Efficiency $V_{IN}$: 240V, Freq: 60Hz**

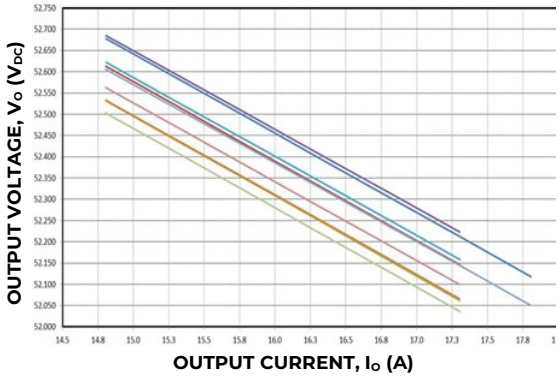



**Figure 2. Output current limit profile (0° - 50°C)**

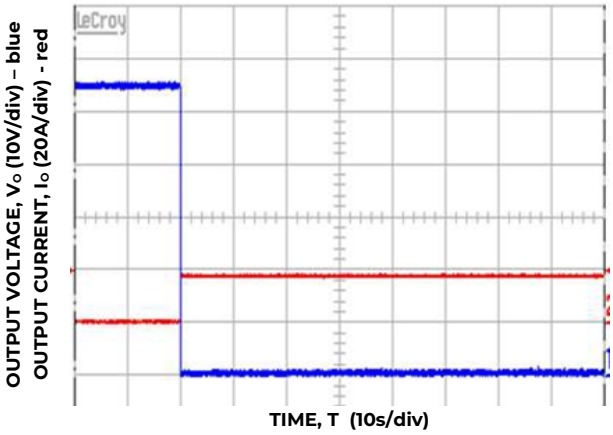



**Figure 3. Short circuit Performance**

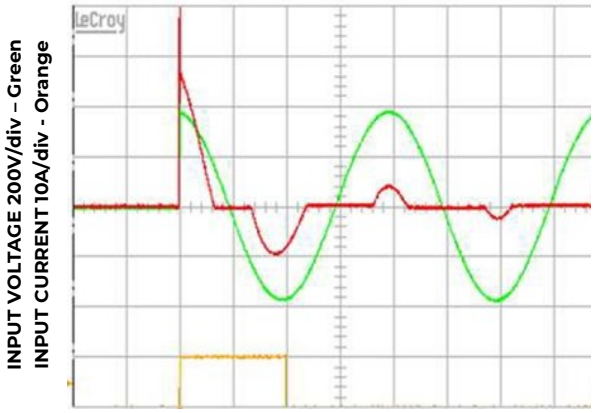



**Figure 4. Inrush performance**

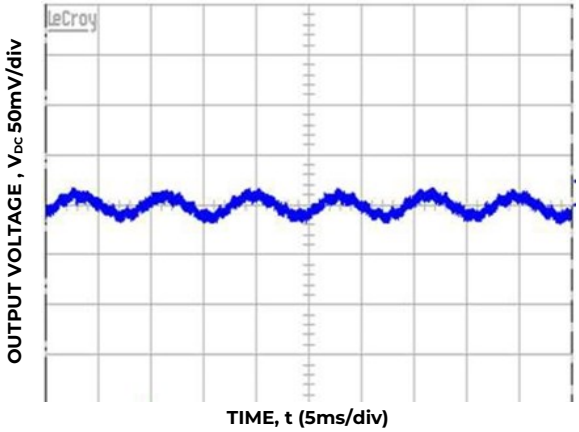



**Figure 5. 54$V_{DC}$ output PARD, full load, $V_{IN}$ = 230$V_{AC}$**

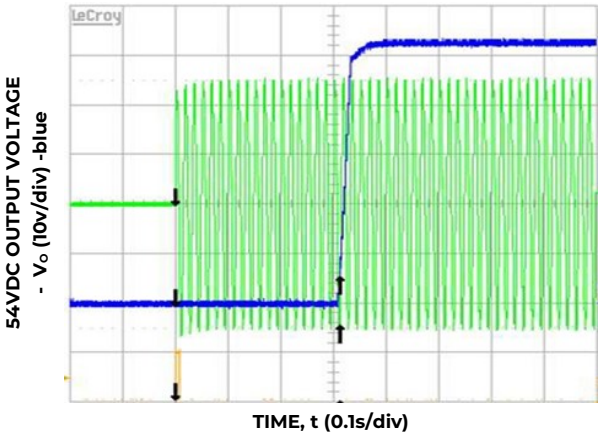



**Figure 6. Start up $V_{IN}$ 176 $V_{AC}$**

## Characteristic Curves (continued)

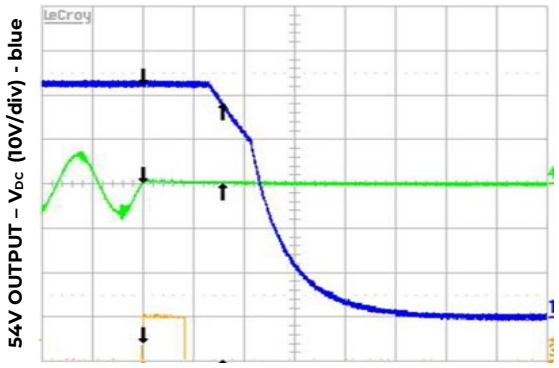



Figure 7. Holdup $V_{IN}$ – 90$V_{AC}$

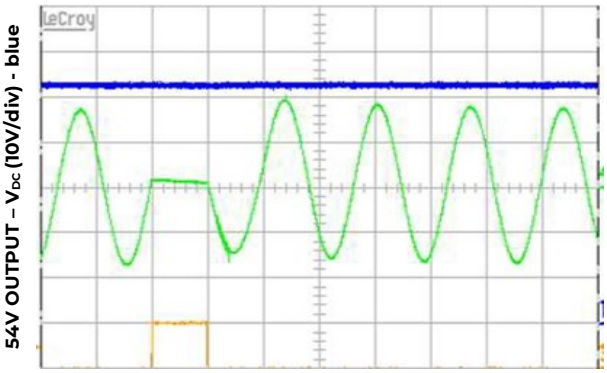



Figure 8. ½ cycle ride-through $V_{IN}$ 240 $V_{AC}$

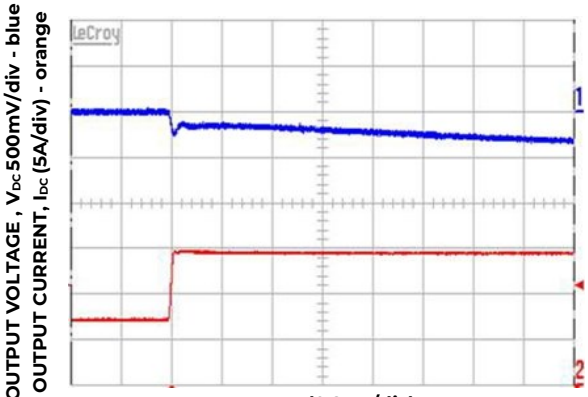



Figure 9. 54V Transient response 50% load step (50 – 100%)

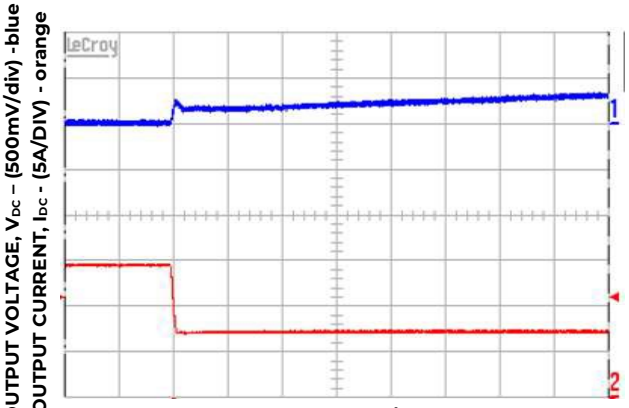



Figure 10. 54V Transient response 50% load step (100 – 50%)

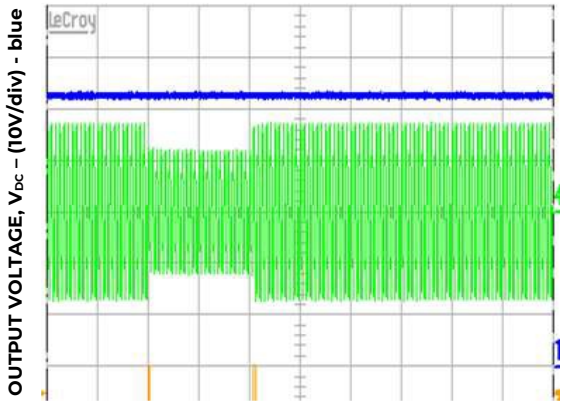



Figure 11. 30% dip ride-through $V_{IN}$ 240 $V_{AC}$

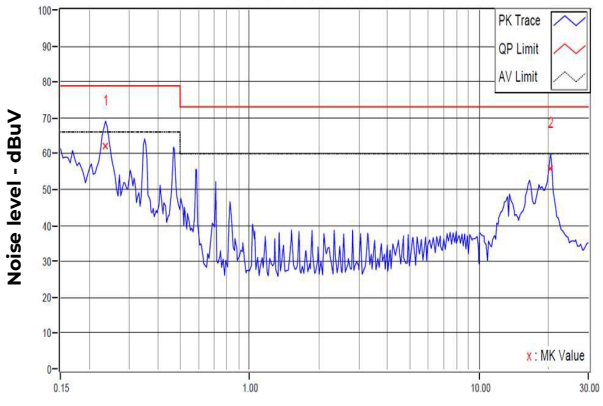



Figure 12. Conducted Emissions

## Control and Status

**Analog controls:** Details of analog controls are provided in this Technical Requirement under Signal Definitions.

**Separate isolated grounds:** The +54$V_{DC}$ output is referenced to its own Output Return. The +12$V_{DC}$ and +3.3$V_{DC}$ are referenced to Signal return.

**POE isolation:** The main 54$V_{DC}$ output is fully isolated from the rest of the power supply, complying with the POE isolation requirements of IEEE802.3af.

## Control Signals

**Module_Enable_L:** This is a short signal pin that controls the presence of the 54$V_{DC}$ main output. This pin should be connected to 'signal return' on the system side of the output connector. The purpose of this pin is to ensure that the output turns ON after engagement of the power blades and turns OFF prior to disengagement of the power blades.

## Status signals

**AC_OK_L:** A TTL compatible status signal representing whether the input voltage is within the anticipated range. This signal needs to be pulled HI externally through a resistor. This signal asserts LO at least 5ms prior to the 54$V_{DC}$ output voltage decaying below 43$V_{DC}$ . The signal shall not assert for a minimum of 10ms after loss of AC power

**DC_OK_L:** A TTL compatible status signal representing whether the output voltage is present. This signal needs to be pulled HI externally through a resistor.

**TEMP_OK_L:** A TTL compatible status signal representing whether an over temperature exists. This signal needs to be pulled HI externally through a resistor. If an over temperature should occur, this signal would pull LO for approximately 10 seconds prior to shutting down the power supply. The unit would restart if internal temperatures recover within normal operational levels. At that time the signal reverts back to its open collector (HI) state.

**PS_PRESENT_L:** This pin is connected to 'Signal_Return' within the power supply. Its intent is to indicate to the system that a power supply is present. This signal may need to be pulled HI externally through a resistor.

## Serial Bus Communications

The I²C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I²C Serial bus.

All signals are referenced to 'Signal_Return'.

**Device addressing:** The microcontroller (MCU) and the EEPROM have the following addresses:

| Device | Address | Address Bit Assignment (Most to Least Significant) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| MCU | 0xBx | 1 | 0 | 1 | 1 | A2 | A1 | A0 | R/W |
| Broadcast | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Address lines (A2, A1, A0):** These signal pins allow up to eight (8) modules to be addressed on a single I²C bus. The pins are pulled HI internal to the power supply. For a logic LO these delay pins should be connected to 'Output Return'

**Serial Clock (SCL):** The clock pulses on this line are generated by the host that initiates communications across the I²C Serial bus. This signal is internally pulled -up to 3.3V via a 1.2kΩ resistor.

**Serial Data (SDA):** This line is a bi-directional data line. This signal is internally pulled-up to 3.3V via a 1.2kΩ resistor.

## Digital Feature Descriptions

PMBus™ compliance: The power supply is fully compliant to the Power Management Bus (PMBus™) rev1.2 require ments.

**Master/Slave:** The 'host controller' is always the MASTER. Power supplies are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

**Clock stretching:** The 'slave' µController inside the power supply may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the power supply.

Note that clock stretching can only be performed after completion of transmission of the 9$^{th}$ ACK bit, the exception being the START command.

### Clock stretching (continued)

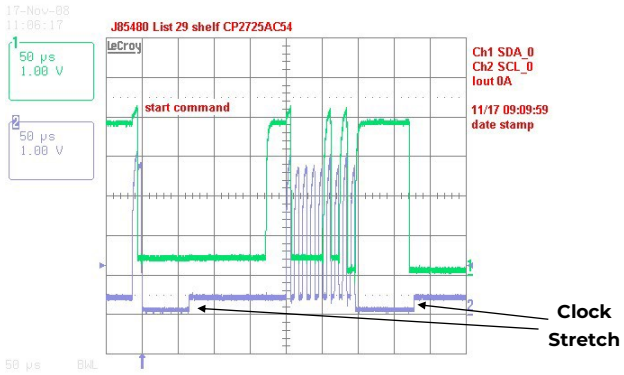



**Figure 1. Example waveforms showing clock stretching.**

**I²C Bus Lock-Up detection:** The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

**Communications speed:** Both 100kHz and 400kHz clock rates are supported. The power supplies default to the 100kHz clock rate. The minimum clock speed specified by SMBus is 10 kHz.

**Packet Error Checking (PEC):** Although the power supply will respond to commands with or without the trailing PEC, it is highly recommended that PEC be used in all communications. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that should require validation to ensure that the correct command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial C (x) = $x^8 + x^2 + x + 1$, in compliance with PMBus™ requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the

**Global broadcast:** This is a powerful command because it can instruct all power supplies to respond simultaneously in one command. But it does have a serious disadvantage. Only a single power supply needs to pull down the ninth acknowledge bit. To be certain that each power supply responded to the global instruction, a READ instruction should be executed to each power supply to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

**Read back delay:** The power supply needs at least 2 seconds to configure the status registers into their final state. For example, a 200 millisecond delay may be required prior to reading back status information after a clear_faults has been issued to clear the status registers.

## PMBus™ Commands

**Standard instruction:** Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is optional and includes the address and data fields.

| 1 | 8 | | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command Code | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| Low data byte | A | High data byte | A | PEC | A | P |

Master to Slave  Slave to Master

SMBUS annotations; S – Start , Wr – Write, Sr – re-Start, Rd – Read, A – Acknowledge, NA – not-acknowledged, P – Stop

**Standard READ:** Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields. PEC is optional and includes the address and data fields.

| 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| S | Slave address | Wr | A | Command Code | A |

| 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|
| Sr | Slave Address | Rd | A | LSB | A |

| 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|
| MSB | A | PEC | No-ack | P |

**Block instruction:** When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands must be used instead of the Standard Instructions.

**Block write format:**

| 1 | 7 | 1 | 1 | | 8 | 1 |
|---|---|---|---|---|---|---|
| S | Slave address | Wr | A | | Command Code | A |

| 8 | 1 | 8 | 1 | 8 | | 1 |
|---|---|---|---|---|---|---|
| Byte count = N | A | Data 1 | A | Data 2 | | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| ..... | A | Data 48 | A | PEC | A | P |

# Technical Specifications (continued)

**Block instruction (continued)**

| 1 | 7 | 1 | 1 | | 8 | 1 |
|---|---|---|---|---|---|---|
| S | Slave address | Wr | A | | Command Code | A |

| 1 | 7 | 1 | 1 |
|---|---|---|---|
| Sr | Slave Address | Rd | A |

| 8 | 1 | 8 | 1 | 8 | | 1 |
|---|---|---|---|---|---|---|
| Byte count = N | A | Data 1 | A | Data 2 | | A |

| 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| ..... | A | Data 48 | A | PEC | NoAck | P |

**Linear Data Format:** The definition is identical to Part II of the PMBus Specification. All standard PMBus values, with the exception of output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16 bit mantissa. Output voltage has a E=9 constant exponent.

The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

| | Data Byte High | | | | | | | | Data Byte Low | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | Exponent (E) | | | | | Mantissa (M) | | | | | | | | | | |

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

$$V = M * 2^{E}$$

Where:

V is the value

M is the 11-bit, two's complement mantissa

E is the 5-bit, two's complement exponent

**PMBus™ Command set:**

| Command | Hex Code | Data Byte | Default State |
|---|---|---|---|
| Operation | 0x01 | 1 | |
| ON_OFF_config | 0x02 | 1 | 0x09, output ON |
| Clear_faults | 0x03 | 0 | |
| Write_protect | 0x10 | 1 | 0x80 |
| Store_default_all | 0x11 | 0 | |
| Restore_default_all | 0x12 | 0 | |
| Capability | 0x19 | 1 | 0x30, 400kHz |
| Vout_mode | 0x20 | 1 | 0x17, N=9 |
| Fan_command_1 | 0x3B | 2 | In RPM (linear format) |
| Vout_OV_warn_limit | 0x42 | 2 | |
| Vout_UV_warn_limit | 0x43 | 2 | |
| Vout_UV_fault_limit | 0x44 | 2 | |
| Vout_UV_fault_response | 0x45 | 1 | 0x00, hardware triggered |
| Iout_OC_warn_limit | 0x4A | 2 | |
| OT_fault_limit | 0x4F | 2 | |
| OT_fault_response | 0x50 | 1 | 0XC0 |
| OT_warn_limit | 0x51 | 2 | |
| UT_warn_limit | 0x52 | 2 | |
| UT_fault_response | 0x54 | 1 | 0x00 |
| | | | |
| Status_byte | 0x78 | 1 | |
| Status_word | 0x79 | 2 | |
| Status_Vout | 0x7A | 1 | |
| Status_Iout | 0x7B | 1 | |
| Status_input | 0x7C | 1 | |
| Status_temperature | 0x7D | 1 | |
| Status_CML | 0x7E | 1 | |
| Status_other | 0x7F | 1 | |
| Status_mfr_specific | 0x80 | 1 | |
| Status_fan_1_2 | 0x81 | 1 | |
| | | | |
| Read_Vout | 0x8B | 2 | |
| Read_Iout | 0x8C | 2 | |
| Read_temperature | 0x8D | 2 | |
| Read_fan_speed_1 | 0x90 | 2 | |
| Read_Pout | 0x96 | 2 | |
| | | | |
| PMBus revision | 0x98 | 1 | |
| Mfr_ID | 0x99 | 5 | FRU_ID |
| Mfr_model | 0x9A | 15 | |
| Mfr_revision | 0x9B | 4 | |
| Mfr_location | 0x9C | 4 | |
| Mfr_date | 0x9D | 6 | |
| Mfr_serial | 0x9E | 15 | |
| Mfr_Vin_min | 0xA0 | 2 | |
| Mfr_Vin_max | 0xA1 | 2 | |
| Mfr_Iin_max | 0xA2 | 2 | |
| Mfr_Pin_max | 0xA3 | 2 | |
| Mfr_Vout_min | 0xA4 | 2 | |
| Mfr_Vout_max | 0xA5 | 2 | |
| Mfr_Iout_max | 0xA6 | 2 | |
| Mfr_Pout_max | 0xA7 | 2 | |
| Mfr_Tambient_max | 0xA8 | 2 | |
| Mfr_Tambient_min | 0xA9 | 2 | |
| User_data_00 | 0xB0 | 48 | User memory space |
| User_data_01 | 0xB1 | 48 | User memory space |
| FRW_revision | D0 | 1 | |

**Status Register Bit Allocation:**

| Register | Hex Code | Data Byte | Function |
|---|---|---|---|
| Status_Byte | 78 | 7 | Busy |
| | | 6 | DC_ OFF |
| | | 5 | Output OV Fault detected |
| | | 4 | Output OC Fault detected |
| | | 3 | Input UV Fault detected |
| | | 2 | Temp Fault/warning detected |
| | | 1 | CML (communication |
| | | 0 | None of Below |
| Status_word (includes Status_byte) | 79 | 7 | OV Fault/Warning detected |
| | | 6 | OC Fault/Warning detected |
| | | 5 | Input Fault/Warning detected |
| | | 4 | Mfr_specific register change detected |
| | | 3 | DC_OFF |
| | | 2 | Fan Fault or Warning detected |
| | | 1 | Other fault |
| | | 0 | Unknown |
| Status_Vout | 7A | 7 | Vout OV Fault |
| | | 6 | Vout OV Warning |
| | | 5 | Vout UV Warning |
| | | 4 | Vout UV Fault |
| | | 3 | N/A |
| | | 2 | N/A |
| | | 1 | N/A |
| | | 0 | N/A |
| Status_Iout | 7B | 7 | IOUT OC Fault |
| | | 6 | N/A |
| | | 5 | IOUT OC Warning |
| | | 4 | N/A |
| | | 3 | N/A |
| | | 2 | N/A |
| | | 1 | N/A |
| | | 0 | N/A |
| Status_input | 7C | 7 | Vin OV Fault |
| | | 6 | Vin OV Warning |
| | | 5 | Vin UV Warning |
| | | 4 | Vin UV Fault |
| | | 3 | N/A |
| | | 2 | N/A |
| | | 1 | N/A |
| | | 0 | N/A |
| Status_temperature | 7D | 7 | OT Fault |
| | | 6 | OT Warning |
| | | 5 | N/A |
| | | 4 | N/A |
| | | 3 | N/A |
| | | 2 | N/A |
| | | 1 | N/A |
| | | 0 | N /A |
| Status_cml | 7E | 7 | Invalid/Unsupported Command |
| | | 6 | Invalid/Unsupported Data |
| | | 5 | Packet Error Check Failed |
| | | 4 | Memory Fault Detected |
| | | 3 | Processor Fault Detected |
| | | 2 | Reserved |
| | | 1 | Other Communications Fault |
| | | 0 | Other Memory or Logic Fault |
| Status_mfr_ specific | 80 | 7 | IDC-OK |
| | | 6 | OVSH# |
| | | 5 | INT# |
| | | 4 | FAULT# |
| | | 3 | OT# |
| | | 2 | DC_OK |
| | | 1 | AC_OK |
| | | 0 | LINE# |
| Status_fan_1_2 | 81 | 7 | Fan_1_fault |
| | | 6 | N/A |
| | | 5 | N/A |
| | | 4 | N/A |
| | | 3 | Fan 1 Speed Overridden |
| | | 2 | N/A |
| | | 1 | N/A |
| | | 0 | N/A |

## Command Descriptions

**Operation (0x01) :** By default the Power supply is turned ON at power up as long as Power ON/OFF signal pin is active HI. The Operation command is used to turn the Power Supply ON or OFF via the PMBus. The data byte below follows the OPERATION command.

| FUNCTION | DATA BYTE |
|---|---|
| Unit ON | 80 |
| Unit OFF | 00 |

To RESET the power supply cycle the power supply OFF, wait at least 2 seconds, and then turn back ON. All alarms and shutdowns are cleared during a restart.

**Clear_faults (0x03):** This command clears all STATUS and FAULT registers.

If a fault still persists after the issuance of the clear_faults command the specific registers indicating the fault are reset again.

**WRITE_PROTECT register (0x10):** Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported command parameters may have their parameters read, regardless of the write_protect settings. The contents of this register can be stored to non-volatile memory using the Store_default_code command. The default setting of this register is disable_all_writes except write_protect 0x80h.

| FUNCTION | DATA BYTE |
|---|---|
| Enable all writes | 00 |
| Disable all writes except write_protect | 80 |
| Disable all writes except write_protect and OPERATION | 40 |

**Vout_OV_warn_limit (0x42):** OV_warning is extremely useful because it gives the system controller a heads up that the output voltage is drifting out of regulation and the power supply is close to shutting down. Pre-amative action may be taken before the power supply would shut down and potentially disable the system.

**Vout_OV_fault_response (0x41):** The power supply can be programmed to latch at a level set by Vout_OV_fault_limit by changing the response to 0x40.

**Vout_UV_fault_response (0x45):** The power supply can be programmed to latch at a level set by Vout_UV_fault_limit by changing the response to 0x40.

**OT_fault_ response (0x50):** The power supply can be programmed to either resume operation (0xC0) or latch (0x40) at a level set vy OT_fault_limit.

**Restart after a latch off:** Either of four restart possibilities are available. The hardware pin Remote ON/OFF may be turned OFF and then ON. The unit may be commanded to restart via i2c through the Operation command by first turning OFF then turning ON . The third way to restart is to remove and reinsert the unit. The fourth way is to turn OFF and then turn ON ac power to the unit. The fifth way is by changing firmware from latch off to restart. Each of these commands must keep the power supply in the OFF state for at least 2 seconds, with the exception of changing to restart.

A power system that is comprised of a number of power supplies could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual power supplies. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all power supplies
2. Toggling Off and then ON the Remote ON/OFF signal
3. Removing and reapplying input commercial power to the entire system

The power supplies should be turned OFF for at least 20 –30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual power supplies.

**Auto_restart:** Auto-restart is the default configuration for recovering from over-current and over-temperature shutdowns. An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again.

**Status_word (0x79):** returns two bytes of information. The upper byte bit functionality is tabulated in the Status_word section. The lower byte bit functionality is identical to Status_byte.

**Invalid commands or data:** The power supply notifies the MASTER if a non-supported command has been sent or inv lid data has been received. Notification is implemented by setting the appropriate STATUS and ALARM registers.

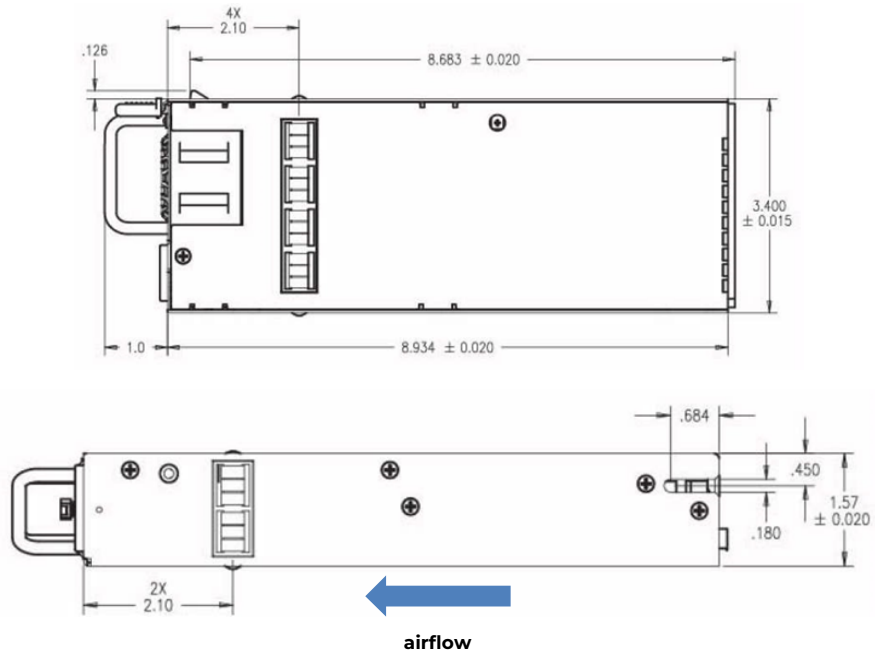
## LEDs

Two LEDs are located on the front faceplate. The AC_OK LED provides visual indication of the INPUT signal function. When the LED is ON GREEN the power supply input is within normal design limits. The second LED is the DC_OK LED. When solid GREEN there are no faults and DC output is present. When blinking GREEN there is an apparent engagement problem with the output connector.

## Alarm Table

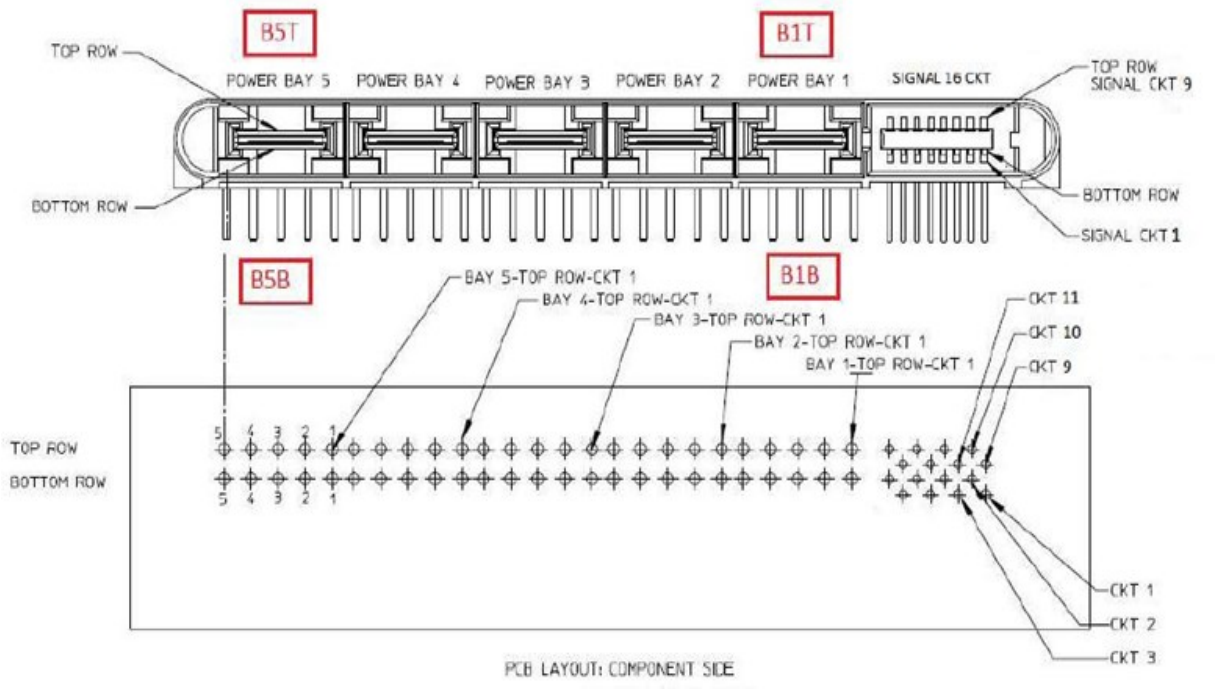
| | Test Condition | LED Indicator | | Monitoring Signals | | |
|---|---|---|---|---|---|---|
| | | LED1 AC_OK | LED2 DC_OK | DC_OK_L | AC_OK_L | TEMP_OK_L |
| 1 | Normal Operation | Green | Green | Low | Low | Low |
| 2 | Low or NO INPUT | Off | Off | High | High | High |
| 3 | OVP | Green | Off | High | Low | Low |
| 4 | Over Current | Green | Off | High | Low | Low |
| 5 | Fault Over Temp | Green | Off | High | Low | High |
| 6 | Engagement problem | Green | Blink | High | High | High |

## Outline Drawing



## Connector Pin Assignments

**Input Mating Connector:** IEC320, C13 type
**Output Connector:** Molex P/N: LPH 45985-1423
**Mating connector:** Molex PN # 45984-1422




| Power Circuits | | | |
|---|---|---|---|
| **Bay** | **Function** | **Bay** | **Function** |
| B1T | +12V Fan Power | B1B | Signal_Return |
| B2T | Chassis Ground | B2B | Chassis Ground |
| B3T | Isolation Barrier | B3B | Isolation Barrier |
| B4T | +54V Output | B4B | Output_Return |
| B5T | +54V Output | B5B | Output_Return |

| Signal Circuits | | | |
|---|---|---|---|
| **Pin** | **Function** | **Pin** | **Function** |
| 1 | n/a | 9 | n/a |
| 2 | A0 | 10 | 3.3V[7] |
| 3 | TEMP_OK_L | 11 | A2 |
| 4 | A1 | 12 | SDA |
| 5 | AC_OK_L | 13 | Signal_Return |
| 6 | Signal_Return | 14 | SCL |
| 7 | DC_OK_L | 15 | Signal Return |
| 8 | PS_PRESENT_L | 16 | MODULE_ ENABLE_L |

Note: Signal pins are shorter than power blades in order to ensure that they achieve the last-to-make, first-to-break feature for hot plug

[7] The 3.3V output is for internal use only. This signal pin is to be used only for monitoring purposes.

## Ordering Information

Please contact your OmniOn Power Sales Representative for pricing, availability and optional features.

| PRODUCT | DESCRIPTION | PART NUMBER |
|---|---|---|
| 800W Rectifier | +54$V_{OUT}$, +12$V_{DC}$, PMBus interface, RoHS 6 of 6, airflow rear-to-front | MPR0854FPXXXZ01A |

## Contact Us

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## Change History (excludes grammar & clarifications)

| Revision | Date | Description of the change |
|---|---|---|
| 4.3 | 12/13/2021 | Updated as per template |
| 4.4 | 06/22/2023 | Units are corrected in graph on pages-7/8 |
| 4.5 | 10/23/2023 | Updated as per OmniOn template |

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