GP100H3M50TEZ-FB Global Platform Line High Efficiency Rectifier

3Φ-380/480V_{AC} Input; Default Outputs: ±50V_{DC} @ 6000W, 5V_{DC} @ 3.75W

RoHS Compliant

Description

The GP100 series of rectifiers provide significant efficiency improvements in the Global Platform of Power supplies. High-density front-to-back airflow is designed for minimal space utilization and is highly expandable for future growth. The 3Φ - 380/480V_{rms} input product is designed to be deployed internationally. It is configured with dual-redundant PMBus™ compliant I^2C communications busses that allow it to be used in a broad range of applications. Feature set flexibility makes these rectifiers an excellent choice for applications requiring modular, very-high-efficiency AC to -48V_{DC} intermediate voltages, such as in distributed power.

Applications

- 48V_{DC} distributed power architectures
- Power amplifier
- Routers/ VoIP/Soft and other Telecom Switches
- LAN/WAN/MAN applications
- File servers, Enterprise Networks, Indoor wireless
- SAN/NAS/iSCSI applications
- Semiconductor Manufacturing

Features

- High Efficiency 95.8% typical
- Compact 1RU form factor with 30 W/in^3 density
- Constant power from 48 – 58V_{DC}
- 6000W from nominal 3Φ-380/480V_{AC}
- Output voltage programmable from 18V – 58V_{DC}
- PMBus compliant dual, redundant I^2C serial bus
- Power factor correction (meets EN/IEC 61000-3-2 and EN 60555-2 requirements)
- SEMI-F47 Tested and Compliant
- Output overvoltage and overload protection
- AC Input overvoltage and undervoltage protection
- Over-temperature warning and protection
- Redundant, parallel operation with active load sharing
- Redundant +5V @ 0.75 Aux power
- Remote ON/OFF
- Internally controlled Variable-speed fan
- Hot insertion/removal (hot plug)
- Three front panel LED indicators
- EN/IEC/UL/CSA C22.2 62368-1 2nd edition +A1
- CE mark§
- Meets FCC part 15, EN55032 Class A standards
- Meets EN61000 immunity and transient standards
- Shock & vibration: Meets IPC 9592 Class II standards
- Compliant to RoHS Directive 2011/65/EU and amended Directive (EU) 2015/863.
- Compliant to REACH Directive (EC) No 1907/2006

See footnotes on page 34

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Symbol	Min	Max	Unit
Input Voltage: Continuous	V_{IN}	0	600	V_{AC}
Operating Ambient Temperature[1]	T_A	-10	75	°C
Storage Temperature	T_{stg}	-40	85	°C
I/O Isolation voltage to Frame (100% factory Hi-Pot tested)			2087	V_{AC}

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, V_o=50V_{DC}, resistive load, and temperature conditions. To meet measurement accuracy a warm up time of 1hr may be required.

INPUT

Parameter		Symbol	Min	Typ	Max	Unit
Operating Voltage Range (3Φ delta with safety frame ground)		V_{IN}	320	380/480	530	V_{AC}
Low voltage	Turn-Off	V_{IN}	300		320	
	Turn-On		315		330	
	Hysteresis		5			
High voltage	Turn-Off	V_{IN}	530		550	
	Turn-On		520		545	
	Hysteresis		5			
Input voltage phase unbalance		V_{IN}	-15		10	%
Frequency		F_{IN}	47		63	Hz
Operating Current (3Φ - all phases operational)		I_{IN}			15	A_{AC}
Input current phase unbalance [Po> 3KW]					5	%
Inrush Transient (per Φ at 480V_{RMS}, 25°C, excluding X-Capacitor charging)		I_{IN}		25	30	A_{PK}
Source Impedance (NEC allows 2.5% of source voltage drop inside a building)			0.20	0.25		Ω
Idle Power (at 480V_{AC},25°C)	Main output OFF	P_{IN}		15		W
	Main output ON @ Io=0			25		
Leakage Current (per Φ, 530V_{AC}, 60Hz)[2]		I_{IN}			7.8	mA
Power Factor (output power>3KW)		PF	0.96	0.995		
Efficiency (380/480V_{AC} , 50V V_o @ 25°C)	10% load 20% load 50% load 100% load	η		90/90 93.5/92.3 95.5/95.8 94.5/95.4		%
Holdup time (V_{in} = 320V_{AC}, 50Vset, V_{out} decays to 42V_{DC}, 70% load)		T	10			ms
Ride through (480V_{AC}, 25°C, 50V, 100% full load 380V_{ac}, 50V, 70% full load)		T	1/2			cycle
Isolation (per EN62368)	Input – Output	V	3000			V_{AC}
	Input-Chassis/Signals		2000			V_{AC}

See footnotes on page 34

Electrical Specifications (continued)

MAIN OUTPUT

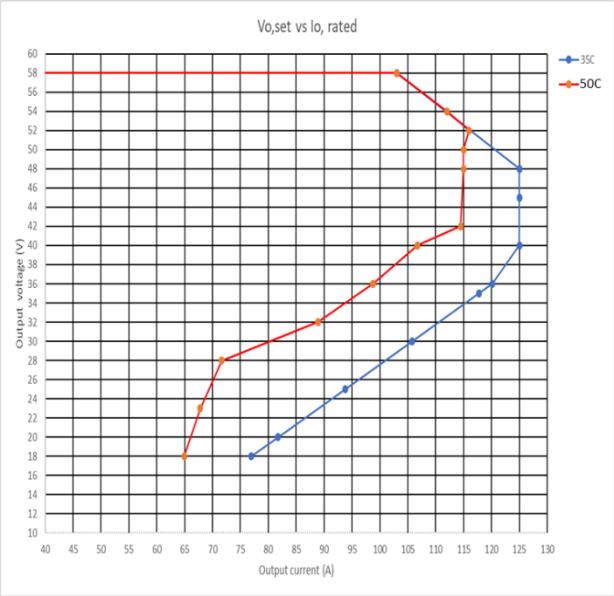
Parameter		Symbol	Min	Typ	Max	Unit
Output Power (320 – 530V_{AC} – 3Φ, T_{AMB}= -5– 45°C , V_o≥48V_{dc})		W	6000			W_{DC}
Factory set default set point V_{IN} = 380V/480V, I = 10% FL, 25°C Nominal set point (droop regulation; max-no load, min-full load)		V_{OUT}	-550	50	+50	V_{DC} mV_{DC}
Overall regulation (load, temperature, aging) 0 – 45°C LOAD > 2.5A, V_o≥42V T_{AMB} > 45°C			-1 -2		+1 +2	% %
Output Voltage Set Range			18		58	V_{DC}
Output Current (T_{AMB} = 45°C)	V_{OUT} = 54V_{DC} V_{OUT} = 50V_{DC} V_{OUT} = 48V_{DC}	I_{Out}	1 1 1		111 120 125	A_{DC}
Current Share (> 50% FL)	>42V active current share <42V active current share		-5 -10		5 10	%FL
Output Ripple (20MHz bandwidth)	RMS (5Hz to 20MHz) Peak-to-Peak (5Hz to 20MHz)	V_{OUT}			100 600	mV_{rms} mV_{p-p}
External Bulk Load Capacitance		C_{OUT}	0		1,700	µF/A
Turn-On (monotonic turn-ON from 30 – 100% of V_{nom}, above -5°C[3]) AC input Turn-on Delay[4] Remote Turn-on Delay[5] Rise Time – PMBus or Analog mode		T		5 280 100	 500	S Ms ms
Output Overshoot		V_{OUT}			2	%
Load Step Response ΔI [V_{IN} = 380/480V_{AC}, 25°C, load step 20% « 80% FL[6], di/dt = 1A/µs]		I_{OUT}			60	%FL
ΔV, (380/480 V_{AC}, 25°C)		V_{OUT}	-2		2	V
Settling Time to normal regulation		T			2	Ms
Overload[7] - Power limit when V_{OUT} ≥ 48V_{DC}		P_{OUT}	6050			W_{DC}
Over current protection		Latched off after re-start one time and overcurrent still present.				
System power up		Upon startup, delay overload shutdown for 20 seconds to allow the insertion and startup of multiple modules within a system.				

See footnotes on page 34

Electrical Specifications (continued)

MAIN OUTPUT

Parameter		Symbol	Min	Typ	Max	Unit
Permissible load boundary varies with ambient temperature and $V_{o,set}$. Refer the right curves for load boundary at 35degC and 55degC. 35degC 18 20 25 30 35 36 40 48 58 77 82 94 106 118 120 125 125 103 50degC 18 23 28 32 36 40 42 48 50 52 54 58 65 68 72 89 99 107 114.5 115 115 116 112 103 The overload current limit threshold should be set about at least 1% above the load envelope shown here. Contract terms are for supporting all loads inside the load map. The customer will develop a control interface which maintains the operating voltage and current so as to not exceed the load map. A dynamic OC_LV fault limit is implemented. $V_{o,set} \geq 42V$, OC_LV fault limit is 40V $V_{o,set} < 42V$, OC_LV fault limit is ($V_{o,set}$ -2V)						
Overvoltage	200ms delayed shutdown with default setting[8] Immediate shutdown	V_{OUT}	59 >65	59.5	60	V_{DC}
	Programmable range		44		59.5	
	Latched shutdown	If 3 restart attempted within a 30 sec window unit latches OFF				
	Restart delay		3.5	4	5	sec
	Restart/Reset conditions for latching	Loss of input > 100ms or Output OFF followed by ON command				
Over-temperature warning (prior to commencement of shutdown) Shutdown (below the max device rating being protected) Restart attempt Hysteresis (below shutdown level)		T		5 20 10		°C
Isolation Output-Chassis		V	500			V_{DC}



See footnotes on page 34

Electrical Specifications (continued)

5V_{DC} Auxiliary output

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltage Setpoint	V_{OUT}		5		V_{DC}
Overall Regulation		-5		+5	%
Output Current		0		0.75	A
Rise time			2.2		ms
Turn on early than main power into regulation		450			ms
Ripple and Noise (20MHz bandwidth)			50	100	mV_{p-p}
Over-voltage Clamp				7	V_{DC}
Over-current Limit output drops out of regulation Shutdown			 150 250		 %FL %FL

General Specifications

Parameter		Min	Typ	Max	Units	Notes
Reliability	Calculated		560,000 190,000		Hours	Full load, 25°C ; Full load, 55°C ; - MTBF per Telecordia SR232 Reliability protection for electronic equipment, issue 3, method I, case III,
Service Life			10		Years	80% load, 35°C ambient, excluding fans
Unpacked Weight			4.2/9.4		kg/lbs	
Packed Weight			4.7/10.4		Kg/lbs	
Heat Dissipation		200 Watts or 682 BTUs @ 80% load, 250 Watts or 853 BTUs @ 100% load				

Signal Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. Signals are referenced to Logic_GRD unless noted otherwise.. See the Signal Definitions table for additional information.

Parameter	Symbol	Min	Typ	Max	Unit
Remote ON/OFF (should be connected to Logic_GRD)					
main output OFF	V_{OUT}	2.5	-	12	V_{DC}
main output ON	V_{OUT}	0	-	0.8	V_{DC}
V_{prog}					
Voltage control range	$V_{control}$	0		3.3	V_{DC}
Programmed output voltage range	V_{OUT}	18		58	V_{DC}
Voltage adjustment resolution (12-bit A/D)	$V_{control}$		TBD		mV_{DC}
Output configured to 50V_{DC}[9]	$V_{control}$	3.1		3. 3	V_{DC}
Output configured to 18V_{DC}	$V_{control}$	0		0.1	V_{DC}
Interlock [should be connected externally to Vout (-)]	V	-		0.4	V_{DC}

See footnotes on page 34

Signal Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Module Present [Internally shorted to Logic_GRD] Normal operation	V	-		0.4	V_{DC}
Fault (need to be pulled up externally to V_{stdby}[10]) Logic HI (No fault is present) Sink current Logic LO (Fault is present)	V I V	0.7 V_{stdby} - 0	- - -	V_{stdby} 5 0.4	V_{DC} mA V_{DC}
8V_INT (no components should be connected to this pin) Interconnected between power supplies to back-bias the internal secondary processor					
Power fail warning (need to be pulled up externally to V_{stdby}) Logic HI (No Alert – normal) Sink current Logic LO (Alert is set)	V V	0.7V_{stdby} 0		V_{stdby} 5 0.4	V_{Dc} mA V_{Dc}

Digital Interface Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
PMBus Signal Interface Characteristics[11]						
Input Logic High Voltage (CLK, DATA, SMBALERT)		V	1.5		3.6	V_{DC}
Input Logic Low Voltage (CLK, DATA,SMBALERT)		V	0		0.8	V_{DC}
Input high sourced current (CLK, DATA, SMBALERT)		I	0		10	µA
Output Low sink Voltage (CLK, DATA, SMBALERT#)	I_{OUT}=3.5mA	V			0.4	V_{DC}
Output Low sink current (CLK, DATA, SMBALERT#)		I	3.5			mA
Output High open drain leakage current (CLK,DATA, SMBALERT#)	V_{OUT}=3.6V	I	0		10	µA
PMBus Operating frequency range	Slave Mode	FPMB	10		400	kHz
Measurement System Characteristics						
Clock stretching		$T_{stretch}$			25	ms
Standard measurement parameters	Update frequency Report delay after 25% step Report delay to accuracy				1 2 10	Hz Sec sec
I_{OUT} measurement range	Linear	I_{MR}	0		130	A_{DC}
I_{OUT} measurement accuracy 25°C	> 25A < 25A	$I_{OUT(ACC)}$	-1.5 -2.5		+1.5 +2.5	% of FL A_{DC}
V_{OUT} measurement range	Linear	$V_{OUT(rMR)}$	0		70	V_{DC}
V_{OUT} measurement accuracy[12]		$V_{OUT(ACC)}$	-1		+1	%
Temp measurement range	Linear	$Temp_{(rMG)}$	0		150	°C
Temp measurement accuracy[13]		$Temp_{(ACC)}$	-5		+5	%

See footnotes on page 34

Digital Interface Specifications (continued)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Measurement System Characteristics (continued)						
V_{IN} measurement range, each phase	Linear	$V_{IN(rMG)}$	0		600	V_{AC}
V_{IN} measurement accuracy		$V_{IN(ACC)}$	-1.5		+1.5	%
I_{IN} measurement range, each phase	Linear	$I_{IN(MR)}$	0		20	A_{DC}
I_{IN} measurement accuracy		$I_{IN(ACC)}$	-5		5	% of FL
P_{IN} measurement range, computed 3Φ result	Linear	$P_{in(rng)}$	0		6750	W_{in}
P_{IN} measurement accuracy	Linear	$P_{in(ACC)}$	-200		+200	W
F_{IN} measurement range	Linear	$F_{IN(MR)}$	45		65	Hz
F_{IN} measurement accuracy		$F_{IN(ACC)}$				
Fan Speed measurement range	Linear		0		30k	RPM
Fan Speed measurement accuracy			-10		10	%
Fan speed control – duty cycle	Linear		0		100	%

Environmental Specifications

Parameter		Min	Typ	Max	Units	Notes
Ambient Temperature		-5[14]		50	°C	Air inlet from sea level to 5,000 feet. Refer to load boundary curves with $V_{o,set}$ & ambient temperature
Storage Temperature		-40		85	°C	
Operating Altitude				1524/5000	m / ft	
Non-operating Altitude				8200/30k	m / ft	
Power Derating with Temperature				2.0	%/°C	50°C to 75°C[15]
Power Derating with Altitude				2.0	°C/305 m °C/1000 ft	Above 1524/5000 m/ft; 3962/13000 m/ft max
Humidity	Operating Storage	5 5		95 95	% %	Relative humidity, non-condensing
Shock and Vibration	Operational	Meets IPC 9592 Class II, Section 5 and GR-63_CORE requirements				
	Packaged	0.02	0.01	0.02	g^2/Hz	Modified lASTM-D-4728-91 8 hour duration on each axis
Acoustic Noise			55	58	dBA	
Earthquake Rating		4			Zone	Design to meet GR-63_CORE requirements at system level

See footnotes on page 34

Environmental Specifications

EMC [Surges and sags applied one Φ at a time and all 3Φ's simultaneously; phase angles 0, 90, 270°

Parameter	Function	Standard		Level	Criteria	Test
AC input	Conducted emissions	EN55032, FCC part 15 EN61000-3-2, Telcordia GR1089-CORE		A – 6dB margin		0.15 – 30MHz 0 – 2 KHz
	Radiated emissions[16]	EN55032		A – 6dB margin		30 – 10000MHz
	Line sags and interruptions	EN61000-4-11 Criteria A: Output will stay above $40V_{DC}$ @ full load			A[17]	-30%, 10ms
					B	-60%, 100ms
					B	-100%, 5sec
					A[18] A[19] B	25% sag for 2 sec 1/2 cycle interruption 1 cycle interruption
		SEMI-F47 Compliant at $480V_{ac}$ Output will Stay at Full Power		50% Sag	Any Phase	10 cycles @ 50Hz 12 cycles @ 60Hz
				70% Sag		25 cycles @ 50Hz 30 cycles @ 60Hz
				80% Sag		50 cycles @ 50Hz 60 cycles @ 60Hz
	Lightning surge	EN61000-4-5, Level 4, 1.2/50µs – error free			A	4kV, com
					A	2kV, diff
		ANSI C62.41-2002	100kHz ring wave 1.2/50µs-8/20µs 550ns EFT burst	3, Category B 3, Category B	B, Table 2 B, Table 3 B, Table 7	6kV/0.5kA 6kV, 3kA 2kV, severity II
	Fast transients	EN61000-4-4		3	A	5/50ns, 2kV (common mode)
Enclosure immunity	Conducted RF fields	EN61000-4-6		3	A	130dBµV, 0.15-80MHz, 80% AM
	Radiated RF fields	EN61000-4-3		3	A	10V/m, 80-1000MHz, 80% AM
		ENV 50140			A	
	ESD	EN61000-4-2		4	A	8kV contact, 15kV air

Criteria	Performance
A	No performance degradation
B	Temporary loss of function or degradation not requiring manual intervention
C	Temporary loss of function or degradation that may require manual intervention
D	Loss of function with possible permanent damage

See footnotes on page 34

Control and Status

The Rectifier provides three means for monitor/ control: analog, PMBus™.

Details of analog control and the PMBus™ based protocol are provided in this data sheet.

Control hierarchy: Some features, such as output voltage, can be controlled both through hardware and firmware. For example, the output voltage is controlled both by a signal pin (V_{prog}) and firmware (V_{out}_command, 0x21).

Using output voltage as an example, the V_{prog} signal pin voltage level sets the output voltage if its value is between 0.1 and 3.0 V_{DC} (see the "Voltage programming" section). When the programming signal V_{prog} is > $3V_{DC}$, the output voltage is set at the default value of $50V_{DC}$.

The signal pin controls the corresponding feature until the firmware command is executed. Once the firmware command has been executed, the signal pin is ignored until input power is removed and reapplied, which resets control to the signal pin. In the above example, the rectifier will no longer 'listen' to the V_{prog} pin after V_{out}_command has been executed, as long as input power is applied without interruption.

In summary, hardware signals such as V_{prog} are utilized for setting the initial default value and for varying the value until firmware based control takes over. Once firmware control is executed, hardware based control is relinquished so the processor can clearly decide who has control.

Analog controls: Details of analog controls are provided in this data sheet under Feature Specifications.

Signal Reference: Unless otherwise noted, all signals, the standby output, and I²C communications are referenced to Logic_GRD. See the Signal Definitions Table at the end of this document for further description of all the signals.

Logic_GRD is capacitively coupled to Frame_GRD inside the rectifier. The maximum voltage differential between Logic_GRD and Frame_GRD should be less than $100V_{DC}$. It is assumed that the end user will connect Logic_GRD to his digital ground reference in his system.

Logic_GRD is isolated from the main output of the rectifier.

Control Signals

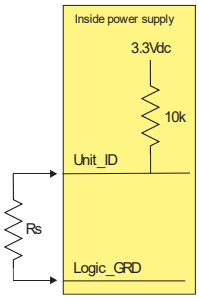
Protocol: This signal pin defines the communications mode setting of the rectifier. Two different states can be configured. State #1 is the I²C application in which case the protocol pin should be left a no-connect. State #2 is the RS485 mode application in which case a resistor value between 1kΩ and 5kΩ should be present between this pin and V_{out} (-).

Device address in I²C mode: Address bits A3, A2, A1, A0 set the specific address of the µP in the rectifier. With these four bits, up to sixteen (16) rectifiers can be independently addressed on a single I²C bus. These four bits are configured by two signal pins, Unit_ID and Rack_ID. The least significant bit x (LSB) of the address byte is set to either write [0] or read [1]. A write command instructs the rectifier. A read command accesses information from the rectifier.

Device	Address	Address Bit Assignments (Most to Least Significant)							
		7	6	5	4	3	2	1	0
µP	40 – 4F	1	0	0	A3	A2	A1	A0	R/W
Broadcast	00	0	0	0	0	0	0	0	0
		MSB							LSB

Unit_ID: Up to 10 different units are selectable.

A voltage divider between 3.3V and Logic_GRD configures Unit_ID. Internally a 10kΩ resistor is pulled up to $3.3V_{DC}$. A pull down resistor Rs needs to be connected between pin Unit_ID and Logic_GRD.



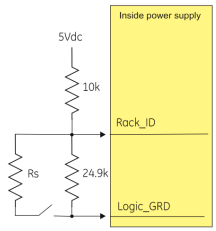
Unit_ID	Voltage level	R_S (± 0.1%)
Invalid	3.30	
1	3.00	100k
2	2.67	45.3k
3	2.34	24.9k
4	2.01	15.4k
5	1.68	10.5k
6	1.35	7.15k
7	1.02	4.99k
8	0.69	2.49k
9	0.36	1.27k
10	0	0

See footnotes on page 34

Technical Specifications (continued)

Rack_ID: Up to 8 different units are selectable.

A voltage divider between $5V_{DC}$ and Logic_GRD configures Rack_ID. A switch between each R_S value changes the Rack_ID level according to the table below.



Rack_ID	Voltage level[20]	5% tolerance	
1	3.31	3. 15	3.48
2	1.07	1.02	1.13
3	1.89	1.80	1.99
4	0.58	0.55	0.60
5	1.66	1.57	1.74
6	0.84	0.80	0.88
7	1.42	1.35	1.49
8	2.86	2.71	3.00

Configuration of the A3–A0 bits: The rectifier will determine the configured address based on the Unit_ID and Rack_ID voltage levels as follows (the order is A3 – A0):

		Unit_ID				
		1	2	3	4	5
Rack_ID	1	0000	0001	0010	0011	
	2	0100	0101	0110	0111	
	3	1000	1001	1010	1011	
	4	1100	1101	1110	1111	
	5					
	6	0000	0001	0010	0011	0100
	7	0101	0110	0111	1000	1001
	8	1010	1011	1100	1101	1110

Unit x Shelf: 4 x 4 and 5 x 3

		Unit_ID				
		6	7	8	9	10
Rack_ID	1	0000	0001			
	2	0010	0011			
	3	0100	0101			
	4	0110	0111	0000	0001	0010
	5	1000	1001	0011	0100	0101
	6	1010	1011	0110	0111	1000
	7	1100	1101	1001	1010	1011
	8	1110	1111	1100	1101	1110

Unit x Shelf: 2 x 8 and 3 x 5

Slot_ID/Interlock: In I^2C mode, the Slot_ID pin must be shorted to $V_{out}(-)$ in order to deliver output power. This connection provides an interlock feature. refer description about interlock feature.

Global Broadcast: This is a powerful command because it instruct all power supplies to respond simultaneously. A read instruction should never be accessed globally. The rectifier should issue an 'invalid command' state if a 'read' is attempted globally.

For example, changing the 'system' output voltage requires the global broadcast so that all paralleled power supplies change their output simultaneously. This command can also turn OFF the 'main' output or turn ON the 'main' output of all power supplies simultaneously. Unfortunately, this command does have a side effect. Only a single rectifier needs to pull down the ninth acknowledge bit. To be certain that each rectifier responded to the global instruction, a READ instruction should be executed to each rectifier to verify that the command properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Voltage programming (V_{prog}): Hardware voltage programming controls the output voltage until a software command to change the output voltage is executed. Software voltage programming permanently overrides the hardware margin setting and the rectifier no longer listens to any hardware margin settings until power to the controller is interrupted, for example if input power or bias power is recycled.

See footnotes on page 34

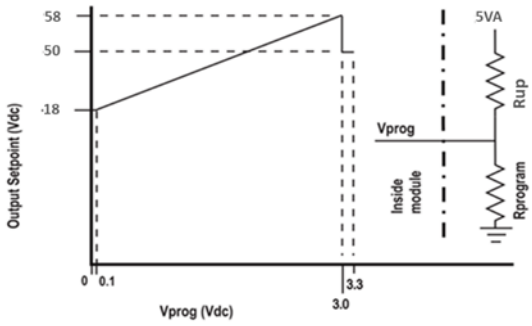
When bias power is recycled to the controller the controller restarts into its default configuration, programmed to set the output as instructed by the V_{prog} pin. Again, subsequent software commanded settings permanently override the margin setting. As an example, applying a voltage between V_{prog} and Logic_GRD is an effective way of changing the factory set point of the rectifier to whatever voltage level is desired by the user during initial start-up.

The V_{prog} pin level should be set by a divider from $3.3V_{dc}$ to Logic_GRD external to the rectifier as shown in the graph. Programming can be accomplished either by a resistor divider or by a voltage source injecting a precision voltage level into the V_{prog} pin. Above $3V_{dc}$ the rectifier sets the output to its default state.

If V_{prog} feature is not used, this signal should be pulled up to 3.3V with a resistor.

An analog voltage on this signal can vary the output voltage from $18V_{dc}$ to $58V_{dc}$.

Note that in RS485 mode this pin is ignored



Factory default setting driven by V_{prog}

Load share (I_{share}): This is a single wire analog signal that is generated and acted upon automatically by power supplies connected in parallel. I_{share} pins should be connected to each other for power supplies, if active current share among the power supplies is desired. No resistors or capacitors should get connected to this pin.

Note that in RS485 mode this pin is ignored

ON/OFF: Controls the main $54V_{DC}$ output when either analog control or PMBus protocols are selected, as configured by the Protocol pin. This pin must be pulled low to turn ON the rectifier. The rectifier will turn OFF if either the ON/OFF or the Interlock pin is released. This signal is referenced to Logic_GRD.

Note that in RS485 mode this pin is ignored.

Interlock: This is a shorter pin utilized for hot-plug applications to ensure that the rectifier turns OFF before the power pins are disengaged. It also ensures that the rectifier turns ON only after the power pins have been engaged. Must be connected to V_OUT (-) for the rectifier to be ON.

8V_INT: Single wire connection between modules, provides redundant bias to the DC/DC control circuitry of an unpowered module.

Status Signals

Module Present: This signal is used as an OUTPUT signal by the rectifier to notify the system controller that a rectifier is physically present in the slot. This signal pin is pulled down to Logic_GRD by the rectifier.

Power fail warning#: This signal is HI when the main output is being delivered and goes LO if the main output is shutdown due to protection or internal fault. PFW# also pulses at a 1ms duty cycle if the unit is in overload.

Fault#: A TTL compatible status signal representing whether a Fault occurred. This signal needs to be pulled HI externally through a resistor. This signal goes LO for any failure that requires rectifier replacement.

Note that in RS485 mode this pin is ignored

These faults may be due to:

- Fan failure
- Over-temperature shutdown
- Over-voltage shutdown
- Internal Rectifier Fault

Serial Bus Communications

The I^2C interface facilitates the monitoring and control of various operating parameters within the unit and transmits these on demand over an industry standard I^2C Serial bus.

All signals are referenced to 'Logic_GRD'.

Pull-up resistors: The clock, data, and Alert# lines do not have any internal pull-up resistors inside the rectifier. The customer is responsible for ensuring that the transmission impedance of the communications lines complies with I^2C and SMBus standards.

See footnotes on page 34

Serial Clock (SCL): The clock pulses on this line are generated by the host that initiates communications across the I²C Serial bus. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C /SMBus specifications.

Serial Data (SDA): This line is a bi-directional data line. This signal needs to be pulled HI externally through a resistor as necessary to ensure that rise and fall time timing and the maximum sink current is in compliance to the I²C /SMBus specifications.

Digital Feature Descriptions

PMBus™ compliance: The rectifier is fully compliant to the Power Management Bus (PMBus™) rev1.2 requirements. This Specification can be obtained from www.pmbus.org.

'Manufacturer Specific' commands are used to support additional instructions that are not in the PMBus™ specification.

All communication over the PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the rectifier.

Non-volatile memory is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory. Only those specifically identified as capable of being stored can be saved. (see the Table of Commands for which command parameters can be saved to non-volatile storage).

Non-supported commands: Non supported commands are flagged by setting the appropriate STATUS bit and issuing an SMBAlert# to the 'host' controller. If a non-supported read is requested the rectifier will return 0x00h for data.

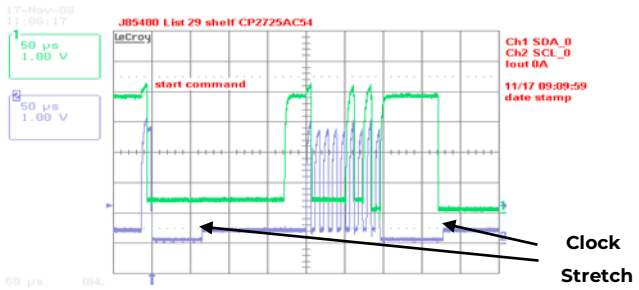
Data out-of-range: The rectifier validates data settings and sets the data out-of-range bit and SMBAlert# if the data is not within acceptable range.

Master/Slave: The 'host controller' is always the MASTER. Power supplies are always SLAVES. SLAVES cannot initiate communications or toggle the Clock. SLAVES also must respond expeditiously at the command of the MASTER as required by the clock pulses generated by the MASTER.

Clock stretching: The 'slave' µController inside the rectifier may initiate clock stretching if it is busy and it desires to delay the initiation of any further communications. During the clock stretch the 'slave' may keep the clock LO until it is ready to receive further instructions from the host controller. The maximum clock stretch interval is 25ms.

The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the rectifier.

Note that clock stretching can only be performed after completion of transmission of the 9th ACK bit, the exception being the START command.



Example waveforms showing clock stretching.

I²C Bus Lock-Up detection: The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

Communications speed: Both 100kHz and 400kHz clock rates are supported. The power supplies default to the 100kHz clock rate.

Packet Error Checking (PEC): The rectifier will not respond to commands without the trailing PEC. The integrity of communications is compromised if packet error correction is not employed. There are many functional features, including turning OFF the main output, that require validation to ensure that the correct command is executed.

PEC is a CRC-8 error-checking byte, based on the polynomial $C(x) = x^8 + x^2 + x + 1$, in compliance with PMBus™ requirements. The calculation is based in all message bytes, including the originating write address and command bytes preceding read instructions. The PEC is appended to the message by the device that supplied the last byte.

See footnotes on page 34

Alert#: The rectifier can issue Alert# driven from either its internal micro controller (µC) or from the I²C bus master selector stage. That is, the Alert# signal of the internal µC funnels through the master selector stage that buffers the Alert# signal and splits the signal to the two Alert# signal pins exiting the rectifier. In addition, the master selector stage signals its own Alert# request to either of the two Alert# signals when required.

The µC driven Alert# signal informs the 'master/host' controller that either a STATE or ALARM change has occurred. Normally this signal is HI. The signal will change to its LO level if the rectifier has changed states and the signal will be latched LO until the rectifier receives a 'clear_faults' instruction.

The signal will be triggered for any state change, including the following conditions;

- V_{IN} under or over voltage
- V_{out} under or over voltage
- I_{OUT} over current
- Over Temperature warning or fault
- Fan Failure
- Communication error
- PEC error
- Invalid command
- Internal faults
- Both Alert#_0 and -1 are asserted during power up to notify the master that a new rectifier has been added to the bus.

The rectifier will clear the Alert# signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR_FAULTS command
- Bias power to the processor is recycled

The rectifier will re-assert the Alert line if the internal state of the rectifier has changed, even if that information cannot be reported by the status registers until a clear_faults is issued by the host. If the Alert asserts, the host should respond by issuing a clear_faults to retire the alert line (this action also provides the ability to change the status registers). This action triggers another Alert assertion because the status registers changed states to report the latest state of the rectifier. The host is now able to read the latest reported status register information and issue a clear_faults to retire the Alert signal.

Re-initialization: The I²C code is programmed to re-initialize if no activity is detected on the bus for 5 seconds. Re-initialization is designed to guarantee that the I²C µController does not hang up the bus. Although this rate is longer than the timing requirements specified in the SMBus specification, it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. During the few µseconds required to accomplish re-initialization the I²C µController may not recognize a command sent to it. (i.e. a start condition).

Read back delay: The rectifier issues the Alert# notification as soon as the first state change occurred. During an event a number of different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive Alert# could be triggered by the transitioning state of the rectifier. In order to avoid successive Alert# s and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an Alert# before executing a read back. This delay will ensure that only the final state of the rectifier is captured.

Successive read backs: Successive read backs to the rectifier should not be attempted at intervals faster than every one second. This time interval is sufficient for the internal processors to update their data base so that successive reads provide fresh data.

Dual Master Control:

Two independent I²C lines provide true communications bus redundancy and allow two independent controllers to sequentially control the rectifier. For example, a short or an open connection in one of the I²C lines does not affect communications capability on the other I²C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' can take over control at any time.

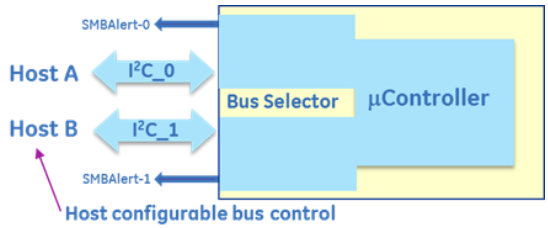
Conceptually a Digital Signal Processor (DSP) referenced to V_{out}(-) of the rectifier provides secondary control. A Bidirectional Isolator provides the required isolation between power GRD, V_{out}(-) and signal GRD (Logic_GRD). A secondary micro controller provides instructions to and receives operational data from the DSP. The secondary micro controller also controls the communications over two independent I²C lines to two independent system controllers.

See footnotes on page 34

The secondary micro controller is designed to default to I²C_0 when powered up. If only a single system controller is utilized, it should be connected to I²C_0. In this case the I²C_1 line is totally transparent as if it does not exist.

If two independent system controllers are utilized, then one of them should be connected to I²C_0 and the other to I²C_1.

At power up the master connected to I²C_0 has control of the bus. See the section on Dual Master Control for further description of this feature.



Conceptual representation of the dual I²C bus system

PMBus™ Commands

Standard instruction: Up to two bytes of data may follow an instruction depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	8	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	A	P

☐ Master to Slave ⬚ Slave to Master

SMBUS annotations; S – Start , Wr – Write, Sr – re-Start, Rd – Read, A – Acknowledge, NA – not-acknowledged, P – Stop

Standard READ: Up to two bytes of data may follow a READ request depending on the required data content. Analog data is always transmitted as LSB followed by MSB. PEC is mandatory and includes the address and data fields.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1	8	1
Sr	Slave address	Rd	A	LSB	A

8	1	8	1	1
MSB	A	PEC	No-ack	P

Block communications: When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands are used instead of the Standard Instructions above to write or read any number of bytes greater than two.

Block write format:

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1	8		1
Byte count = N	A	Data 1	A	Data 2		A

8	1	8	1	8	1	1
.....	A	Data 48	A	PEC	A	P

Block Read format:

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1
Sr	Slave Address	Rd	A

8	1	8	1	8	1
Byte Count = N	A	Data 1	A	Data 2	A

8	1	8	1	8	1	1
.....	A	Data 48	A	PEC	No Ack	P

Linear Data Format: The definition is identical to Part II of the PMBus Specification. All standard PMBus values, with the exception of output voltage related functions, are represented by the linear format described below. Output voltage functions are represented by a 16 bit mantissa. Output voltage has a E=9 constant exponent.

See footnotes on page 34

The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent or scaling factor, its format is shown below.

	Data Byte High								Data Byte Low							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Exponent I					Mantissa (M)										

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

$$V = M * 2^{E}$$

Where: V is the value, M is the 11-bit, two's complement mantissa, E is the 5-bit, two's complement exponent

Standard features

Supported features that are not readable: The commands below are supported at the described setting but they cannot be read back through the command set.

Command	Comments
ON_OFF_CONFIG (0x02)	Both CNTL pin and the OPERATION are supported.
CAPABILITY (0x19)	400KHz, SMBALERT
PMBus revision (0x98)	1.2

Status and Alarm registers: The registers are updated with the latest operational state of the rectifier. For example, whether the output is ON or OFF is continuously updated with the latest state of the rectifier. However, alarm information is maintained until a clear_faults command is received from the host. For example, the shutdown or OC_fault bits stay in their alarmed state until the host clears the registers.

A clear_faults clears all registers. If a fault still persists after the clear_faults is commanded, the register bit annunciating the fault is reset again.

Latched status states until cleared

Shutdown: must be sticky – it tells the customer that the rectifier output has been turned OFF

OV, UV, OC, input, unknown warnings & faults, CML Errors, Internal or External Fault: must be sticky

PMBus™ Command set:

Command	Hex Code	Data Field	Non-Volatile Memory Storage& Default
Operation	0x01	1	Yes/80
Clear_Faults	0x03	-	
Write _Protect	0x10	1	no
Restore_default_all	0x12	-	
Restore_user_all	0x16	-	
Store_user_code	0x17	1	yes
Restore_user_code	0x18	1	
V_{out}_mode	0x20	1	
V_{out}_command	0x21	2	Yes/50
V_{in}_ON	0x35	2	No/320
V_{in}_OFF	0x36	2	No/310
Fan_config_1_2	0x3A	1	no
Fan_command_1	0x3B	2	no
V_{out}_OV_fault_limit	0x40	2	Yes /60
V_{out}_OV_fault_response	0x41	1	No/80
V_{out}_OV_warn_limit	0x42	2	Yes /59
V_{out}_UV_warn_limit	0x43	2	Yes /17
V_{out}_UV_fault_limit	0x44	2	Yes /16
I_{out}_OC_LV_fault_limit	0x48	2	Yes/16
V_{out}_UV_fault_response[21]	0x45	1	No /C0
I_{out}_OC_fault_limit	0x46	2	Yes/126
I_{out}_OC_fault_response	0x47	1	Yes/F8
I_{out}_OC_warn_limit	0x4A	2	Yes/121
OT_fault_limit	0x4F	2	Yes/110
OT_fault_response[22]	0x50	1	Yes/C0
OT_warn_limit	0x51	2	Yes/95
V_{in}_OV_fault_limit	0x55	2	No/540
V_{in}_OV_fault-response	0x56	1	No /C0
V_{in}_OV_warn_limit	0x57	2	Yes/510
V_{in}_UV_warn_limit	0x58	2	Yes/340
V_{in}_UV_fault_limit	0x59	2	No/310
V_{in}_UV_fault_response	0x5A	1	No/C0
Status_byte	0x78	1	
Status_word (+ byte)	0x79	1	
Status_V_{out}	0x7A	1	
Status_I_{out}	0x7B	1	
Status_Input	0x7C	1	
Status_temperature	0x7D	1	
Status_CML	0x7E	1	
Status_fan_1_2	0x81	1	
Read_V_{in}	0x88	2	
Read_I_{in}	0x89	2	
Read_V_{out}	0x8B	2	
Read_I_{out}	0x8C	2	
Read_temp_PFC	0x8D	2	
Read_temp_DC+PRI	0x8E	2	

See footnotes on page 34

	Hex Code	Data Field	Non-Volatile Memory Storage
Read_temp_DC_SEC	0x8F	2	
Read_fan_speed_1	0x90	2	
Read_fan_speed_2	0x91	2	
Read_Pin	0x97	2	
Mfr_ID	0x99	6	
Mfr_model	0x9A	16	
Mfr_revision	0x9B	8	
Mfr_serial	0x9E	16	
Status_summary	0xD0	11	
Status_unit	0xD1	2	
Status_alarm	0xD2	3	
Read_fan_speed	0XD3	6	
Read_input	0xD4	14	
Read_firmware_rev	0xD5	6	
Read_run_timer	0xD6	3	
Status_bus	0xD7	1	
Take over bus control	0xD8		yes
EEPROM Record	0xD9	64	yes
Read_ temp_inlet	0xDB	2	
Reserved for factory use	0XDC		
Reserved for factory use	0XDD		
Reserved for factory use	0XDE		
Test Function	0xDF	1	
Upgrade commands			
Password	0xE0	4	
Target list	0xE1	4	
Compatibility code	0xE2	16	
Software version	0xE3	7	
Memory capability	0xE4	7	
Application status	0xE5	1	
Boot loader	0xE6	1	
Data transfer	0xE7	≤32	
Product comcode	0xE8	11	
Upload_black_box	0xF0	≤32	

Command Descriptions

Operation (0x01) : By default the Rectifier is turned ON at power up as long as Power ON/OFF is active LO. The Operation command is used to turn the Rectifier ON or OFF via the PMBus. The data byte below follows the OPERATION command.

FUNCTION	DATA BYTE
Unit ON	0x80
Unit OFF	0x00

To RESET the rectifier cycle the rectifier OFF, wait at least 2 seconds, and then turn back ON. All alarms and shutdowns are cleared during a restart.

Clear_faults (0x03): Clears all STATUS and FAULT registers and resets the Alert# line of the I²C side in control. The I²C side not in control cannot clear registers in the rectifier. This command is always executable.

If a fault still persists after the issuance of the clear_faults command, the specific registers indicating the fault first clears but then get set again to indicate that the unit is still in the fault state.

WRITE_PROTECT register (0x10): Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. All supported commands may have their parameters read, regardless of the write_protect settings. The contents of this register cannot be stored into non-volatile memory using the Store_user_code command. The default setting of this register is enable_all_writes, write_protect 0x00h. The write_protect command must always be accepted.

FUNCTION	DATA BYTE
Enable all writes	00
Disable all writes except write_protect	80
Disable all writes except write_protect and OPERATION	40

Restore_Default_All (0x12): Restores all register values and responses to the default parameters set in the rectifier. The factory default cannot be changed.

Store_user_code (0x17): Changes the user default setting of a single register. In this fashion some protection is offered to ensure that only those registers that are desired to be changed are in fact changed.

Restore_user_code (0x18): Restores the user default setting of a single register.

See footnotes on page 34

V_{out}_mode (0x20): This is a 'read only' register. The upper three bits specify the supported data format, in this case Linear mode. The lower five bits specify the exponent of the data in two's complement binary format for output voltage related commands, such as V_{out}_command. These commands have a 16 bit mantissa. The exponent is fixed by the module and is returned by this command.

Mode	Bits [7:5]	Bits [4:0] (exponent)
Linear	000b	xxxxxb

V_{out}_Command (0x21) : Used to dynamically change the output voltage of the rectifier. This command can also be used to change the factory programmed default set point of the rectifier by executing a store-user instruction that changes the user default firmware set point.

The default set point can be overridden by the V_{prog} signal pin which is designed to override the firmware based default setting during turn ON.

In parallel operation, changing the output voltage should be performed simultaneously to all power supplies using the Global Address (Broadcast) feature. If only a single rectifier is instructed to change its output, it may attempt to source all the required power which can cause either a power limit or shutdown condition.

Software programming of output voltage permanently overrides the set point voltage configured by the V_{prog} signal pin. The program no longer looks at the 'V_{prog} pin' and will not respond to any hardware voltage settings. If power is removed from the µController it will reset itself into its default configuration looking at the V_{prog} signal for output voltage control. In many applications, the V_{prog} pin is used for setting initial conditions, if different that the factory setting. Software programming then takes over once I^2C communications are established.

To properly hot-plug a rectifier into a live backplane, the system generated voltage should get re-configured into either the factory adjusted firmware level or the voltage level reconfigured by the margin pin. Otherwise, the voltage state of the plugged in rectifier could be significantly different than the powered system.

Voltage margin range: $18V_{DC}$ – $58\ V_{DC}$.

A voltage programming example: The task: set the output voltage to $50.45V_{DC}$

This rectifier supports the linear mode of conversion specified in the PMBus™ specification. The supported output voltage exponent is documented in the V_{out}_mode (0x20) command. The exponent for output voltage setting is 2^{-9} (see the PMBus™ specification for reading this command). Calculate the required voltage setting to be sent; $50.45 \times 2^9 = 25830$. Convert this decimal number into its hex equivalent: 64E6 and send it across the bus LSB first and then MSB; E664 with the trailing PEC.

V_{in}_ON (0x35): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns ON. The default value is $320V_{ac}$.

V_{in}_OFF (0x36): This is a 'read only' register that informs the controller at what input voltage level the rectifier turns OFF. The default value is $310V_{ac}$.

Fan_config_1_2 (0x3A) : This command requires that the fan speed be commanded by duty cycle. Both fans must be commanded simultaneously. The tachometer pulses per revolution is not used. Default is duty cycle control.

Fan_command_1 (0x3B): This command instructs the rectifier to increase the speed of both fans above what is internally required. The transmitted data byte represents the hex equivalent of duty cycle in percentage, i.e. 100% = 0 x 64h. The command can increase or decrease fan speed. An incorrect value will result in a 'data error'.

Sending 00h tells the rectifier to revert back to its internal control.

V_{out}_OV_fault_limit (0x40): Sets the value at which the main output voltage will shut down. The default OV_fault value is set at $60V_{dc}$. This level can be permanently changed and stored in non-volatile memory.

V_{out}_OV_fault_response (0x41): This is a 'read only' register. The only allowable state is a latched state after three retry attempts.

An overvoltage shutdown is followed by three attempted restarts, each successive restart delayed 1 second. If within a 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again. This performance cannot be changed.

See footnotes on page 34

Restart after a latched state: Either of four restart mechanisms is available;

- The hardware pin ON/OFF may be cycled OFF and then ON.
- The unit may be commanded to restart via i^2c through the Operation command by first turning OFF then turning ON .
- The third way to restart is to remove and reinsert the unit.
- The fourth way is to turn OFF and then turn ON ac power to the unit.

A successful restart clears all STATUS and ALARM registers.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

- Issuing a GLOBAL OFF and then a GLOBAL ON command to all rectifiers
- Toggling Off and then ON the ON/OFF signal, if this signal is paralleled among the rectifiers.
- Removing and reapplying input commercial power to the entire system.

The rectifiers should be OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

An overvoltage shutdown is followed by three attempted restarts, each successive restart delayed 1 second. If within a 1 minute window three attempted restarts failed, the unit will latch OFF. If less than 3 shutdowns occur within the 1 minute window then the count for latch OFF resets and the 1 minute window starts all over again. This performance cannot be changed.

V_{out}_OV_warn_limit (0x42): Sets the value at which a warning will be issued that the output voltage is too high. The default OV_warn limit is set at $59V_{dc}$. Exceeding the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

V_{out}_UV_warn_limit (0x43): Sets the value at which a warning will be issued that the output voltage is too low. The default UV_warning limit is set at $17V_{dc}$. Reduction below the warning value will set the Alert# signal. This level can be permanently changed and stored in non-volatile memory.

V_{out}_UV_fault_limit (0x44): Sets the value at which the rectifier will shut down if the output gets below this level. The default UV_fault limit is set at 16Vdc. This register is masked if the UV is caused by interruption of the input voltage to the rectifier. This level can be permanently changed and stored in non-volatile memory.

V_{out}_UV_fault_response (0x45): Sets the response if the output voltage falls below the UV_fault_limit. The default UV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

I_{out}_OC_fault_limit (0x46): Sets the value at which the rectifier will shut down. The default limit is set as 126A. The default level can be permanently changed and stored in non-volatile memory. Which level is changed is contingent on the input voltage applied to the rectifier at the time the change takes place.

I_{out}_OC_fault_response (0x47): Sets the response if the output overload exceeds the OC_Fault_limit value. The default OC_fault_response is hiccup (0xF8). The only two allowable states are latched (0xC0) or hiccup. The default response state can be permanently changed and stored in non-volatile memory. The response is the same for both low_line and high_line operations.

I_{out}_OC_warn_limit (0x4A): Sets the value at which the rectifier issues a warning that the output current is getting too close to the shutdown level. The default limit is 121A. The default level can be permanently changed and stored in non-volatile memory. Which level is changed is contingent on the input voltage applied to the rectifier at the time the change takes place.

Above OC setting is active when V_o is ≥ 42V. Regarding wider V_o application, current limit threshold will be reduced automatically as Vo,set below 42V, refer to $V_{o,set}$ and $I_{o,max}$ for allowed load.

OT_fault_limit (0x4F): Sets the value at which the rectifier responds to an OT event, sensed by the dc-sec

See footnotes on page 34

sensor.. The response is defined by the OT_fault_response register.

OT_fault_response (0x50): Sets the response if the output overtemperature exceeds the OT_Fault_limit value. The default OT_fault_response is hiccup (0xC0). The only two allowable states are latched (0x80) or hiccup. The default response state can be permanently changed and stored in non-volatile memory.

OT_warn_limit (0x51): Sets the value at which the rectifier issues a warning when the dc-sec temperature sensor exceeds the warn limit.

V_{in}_OV_fault_limit (0x55): Sets the value at which the rectifier shuts down because the input voltage exceeds the allowable operational limit. The default V_{in}_OV_fault_limit is set at 540V_{ac}. This level can be permanently lowered and stored in non-volatile memory.

V_{in}_OV_fault_response (0x56): Sets the response if the input voltage level exceeds the Vin_OV_fault_limit value. The default V_{in}_OV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

V_{in}_UV_warn_limit (0x58): This is another warning flag indicating that the input voltage is decreasing dangerously close to the low input voltage shutdown level. The default UV_fault_limit is 340V_{ac}. This level can be permanently raised, but not lowered, and stored in non-volatile memory.

V_{in}_UV_fault_limit (0x59): Sets the value at which the rectifier shuts down because the input voltage falls below the allowable operational limit. The default V_{in}_UV_fault_limit is set at 310V_{ac}. This level can be permanently raised and stored in non-volatile memory

V_{in}_UV_fault_response (0x5A): Sets the response if the input voltage level falls below the V_{in}_UV_fault_limit value. The default V_{in}_UV_fault_response is restart (0xC0). The only two allowable states are latched (0x80) and restart (0xC0). The default response state can be permanently changed and stored in non-volatile memory.

STATUS_BYTE (0x78) : Returns one byte of information with a summary of the most critical device faults.

Bit Position	Flag	Default Value
7	X	0
6	OFF	0
5	V_{OUT} Overvoltage	0
4	I_{OUT} Overcurrent	0
3	V_{IN} Undervoltage	0
2	Temperature	0
1	CML (Comm. Memory Fault)	0
0	None of the above	0

STATUS_WORD (0x79): Returns status_byte as the low byte and the following high_byte.

Bit Position	Flag	Default Value
7	V_{OUT} fault or warning	0
6	I_{OUT} fault or warning	0
5	INPUT	0
4	MFR SPECIFIC	0
3	POWER_GOOD# (is negated)	0
2	FANS	0
1	OTHER	0
0	UNKNOWN	0

STATUS_V_{OUT} (0X7A): Returns one byte of information of output voltage related faults.

Bit Position	Flag	Default Value
7	V_{OUT} OV Fault	0
6	V_{OUT}_OV_WARNING	0
5	V_{OUT}_UV_WARNING	0
4	V_{OUT} UV Fault	0
3-0	X	0

STATUS_I_{OUT} (0X7B): Returns one byte of information of output current related faults.

Bit Position	Flag	Default Value
7	I_{OUT} OC Fault	0
6	X	0
5	I_{OUT} OC Warning	0
4	X	0
3	CURRENT SHARE FAULT	0
2	IN POWER LIMITING MODE	0
1 – 0	X	0

The OC Fault limit sets where current limit is set. The rectifier actually shuts down below the LV fault limit setting.

See footnotes on page 34

STATUS_INPUT (0X7C): Returns one byte of information of input voltage related faults.

Bit Position	Flag	Default Value
7	V_{IN}_OV_Fault	0
6	V_{IN}_OV_Warning	0
5	V_{IN}_UV_ Warning	0
4	V_{IN}_UV_Fault	0
3	Unit OFF for low input voltage	0
2	I_{IN}_OC_Fault	0
1 – 0	X	0

STATUS_TEMPERATURE (0x7D): Returns one byte of information of temperature related faults.

Bit Position	Flag	Default Value
7	OT Fault	0
6	OT Warning	0
5 – 0	X	0

STATUS_CML (0X7E): Returns one byte of information of communication related faults.

Bit Position	Flag	Default Value
7	Invalid/Unsupported Command	0
6	Invalid/Unsupported Data	0
5	Packet Error Check Failed	0
4 – 2	X	0
1	Other Communication Fault	0
0	X	0

STATUS_FAN_1_2 (0x81) : Returns one byte of information with a summary of the most critical device faults.

Bit Position	Flag	Default Value
7	Fan 1 Fault	0
6	Fan 2 Fault	0
5 – 4	Not supported	0
3	Fan 1 speed overwritten	0
2	Fan 2 speed overwritten	0
1 – 0	Not supported	0

Read back Descriptions

Single parameter read back: Functions (except V_{IN}, I_{IN}) can be read back one at a time using the read_word_protocol with PEC. A command is first sent out notifying the slave what function is to be read back followed by the data transfer. Analog data is always transmitted LSB followed by MSB. A NA following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

1	8		1
Sr	Slave address	Rd	A

8	1	8	1	8	1	1
Low data byte	A	High data byte	A	PEC	No-Ack	P

Read back error: If the µC does not have sufficient time to retrieve the requested data, it has the option to return all FF's instead of incorrect data.

Read V_{in}, I_{in} (0x88,0x99): Returns the reading of phase 1.

Read_fan_speed 1 & 2 (0x90, 0x91): Reading the fan speed is in Linear Mode returning the RPM value of the fan.

Read_FRU_ID (0x99,0x9A, 0x9B 0x9E): Returns FRU information. Must be executed one register at a time.

1	8		1	8	1
S	Slave address	Wr	A	Command 0x9x	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = x	A

8	1	8	1	8	1	8	1	1
Byte_1	A	Byte	A	Byte_x	A	PEC	NA	P

See footnotes on page 34

Mfr_ID (0x99): Manufacturer in ASCII – 6 characters maximum,

OmniOn – Critical Power represented as,

OmniOn -CP

Mfr_model (0x9A): Manufacturer model-number in ASCII – 14 characters, for this unit: GP100H3M50TEFB

Mfr_revision (0x9B): Total 8 bytes, provides the product series number when the product was manufactured.

Mfr_serial (0x9E): Product serial number includes the manufacturing date, manufacturing location in up to 16 characters. For example:
13KZ51018193xxx, is decoded as;
13 - year of manufacture, 2013
KZ - manufacturing location, in this case Matamoros
51 - week of manufacture
018193xxx - serial #, mfr choice

Manufacturer-Specific PMBus™ Commands

Many of the manufacturer-specific commands read back more than two bytes. If more than two bytes of data are returned, the standard SMBus™ Block read is utilized. In this process, the Master issues a Write command followed by the data transfer from the rectifier. The first byte of the Block Read data field sends back in hex format the number of data bytes, exclusive of the PEC number, that follows. Analog data is always transmitted LSB followed by MSB. A No-ack following the PEC byte signifies that the transmission is complete and is being terminated by the 'host'.

Mfr_Specific Status and alarm registers: The content and partitioning of these registers is significantly different than the standard register set in the PMBus™ specification. More information is provided by these registers and they are either accessed rapidly, at once, using the 'multi parameter' read back scheme of this document, or in batches of two STATUS and two ALARM registers.

Status_summary (0xD0) : This 'manufacturer specific' command is the basic read back returning STATUS and ALARM register data, output voltage, output current, and internal temperature data in a single read. Internal temperature should return the temperature that is closest to a shutdown level.

1	8		1	8	1
S	Slave address	Wr	A	Command Code	A

1	8		1	8	1
Sr	Slave address	Rd	A	Byte count = 11	A

8	1	8	1	8	1	8	1
Status-2	A	Status-1	A	Alarm-3	A	Alarm-2	A

8	1	8	1	8	1
Alarm-1	A	Voltage LSB	A	Voltage MSB	A

8	1	8	1
Current-LSB	A	Current-MSB	A

8	1	8	1
Temperature-LSB	A	Temperature-MSB	A

8	1	1
PEC	No-Ack	P

Status_unit(0xD1): This command returns the STATUS -2 and STATUS-1 register values using the standard 'read' format.

Bit Position	Flag	Default Value
7	PEC Error	0
6	OC [hiccup=1,latch=0]	1
5	Invalid_Instruction	0
4	Power_Capacity [HL = 1]	x
3	OR'ing Test Failed	0
2	n/a	0
1	Data_out_of_range	0
0	Remote ON/OFF [HI = 1]	x

Status-2

Oring fault: Triggered either by the host driven or'ing test or by the repetitive testing of this feature within the rectifier. A destructive fault would cause an internal shutdown. Success of the host driven test depends on power capacity capability which needs to be determined by the external processor. Thus a non-destructive or'ing fault does not trigger a shutdown.

See footnotes on page 34

Bit Position	Flag	Default Value
7	OT [Hiccup=1, latch=0]	1
6	OR'ing_Test_OK	0
5	Internal_Fault	0
4	Shutdown	0
3	X	0
2	External_Fault	0
1	LEDs_Test_ON	0
0	Output ON (ON = 1)	x

Status-1

Status_alarm (0xD2): This command returns the ALARM-3 - ALARM-1 register values.

Bit Position	Flag	Default Value
7	Interlock open	0
6	Fuse fail	0
5	PFC-DC communications fault	0
4	DC-i²c communications fault	0
3	X	0
2	X	0
1	X	0
0	Or'ing fault	0

Alarm-3

Bit	Flag	Default
7	FAN_Fault	0
6	No_Primary	0
5	Primary_OT	0
4	DC/DC_OT	0
3	V_o lower than BUS	0
2	Thermal sensor filed	0
1	Stby_out_of_limits	0
0	Power_Delivery	0

Alarm-2

Power Delivery: If the difference between sourced current and current share is > 10A, a fault is issued.

Bit	Flag	Default
7	POWER LIMIT	0
6	PRIMARY Fault	0
5	OT_Shutdown	0
4	OT_Warning	0
3	IN OVERCURRENT	0
2	OV_Shutdown	0
1	V_{OUT}_out_of_limits	0
0	V_{IN}_out_of_limits	0

Alarm-1

Over temperature warning: This flag is set 5°C prior to the commencement of an over temperature shutdown.

Read_Fan_speed (0 x D3) : Returns the commanded speed in percent and the measured speed in RPM. If a fan does not exist, or if the command is not supported the unit return 0x00.

The transmitted data byte represents speed in RPM is Linear mode.

The transmitted data byte represents the hex equivalent of duty cycle in percentage, i.e.

100% = 0 x 64h.

1	8	1	8	1
S	Slave address	Wr	A	Command Code	A

1	8	1	8	1
Sr	Slave address	Rd	A	Byte count = 6	A

8	1	8	1	8	1	8	1
Adj%-LSB	A	Adj%-MSB	A	Fan1-LSB	A	Fan1-MSB	A

8	1	8	1	8	1	1
Fan2-LSB	A	Fan2-MSB	A	PEC	No-Ack	P

Read input string (0xD4): Reads back the input voltage, input current and total input power consumed by the rectifier.

See footnotes on page 34

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1
Sr	Slave Address	Rd	A

8	1	8	1	8	1
Byte Count = 14	A	Voltage – LSBΦ1	A	Voltage – MSBΦ1	A

.....	8	1	8	1
	Voltage – LSBΦ3	A	Voltage – MSB-Φ3	A

8	1	8	1
Current – LSB-Φ1	A	Current – MSBΦ1	A

.....	8	1	8	1
	Current – LSBΦ3	A	Current – MSBΦ3	A

8	1	8	1	8	1	1
Power - LSB	A	Power-MSB	A	PEC	No-Ack	P

Read_firmware_rev [0 x D5]: Reads back the firmware revision of all three µC in the module.

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	1	7	1	1	8	1
A	Sr	Slave address	Rd	A	Byte Count = 6	A

8	1	8	1
Primary major rev	A	Primary minor rev	A

8	1	8	1
Secondary major rev	A	Secondary minor rev	A

8	1	8	1	8	1	1
i²c major rev	A	i²c revision	A	PEC	No-ack	P

Read_run_timer [0xD6]: Reads the operational ON state of the rectifier in hours. The operational ON state is accumulated from the time the rectifier is initially programmed at the factory. The rectifier is in the operational ON state both when in standby and when it delivers main output power. Recorded capacity is 10 years

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1	8	1
Sr	Slave Address	Rd	A	Byte count = 3	A

8	1	8	1	8	1
Time – LSB	A	Time	A	Time – MSB	A

8	1	1
PEC	No-ack	P

EEPROM record (0xD9): The µC contains 64 bytes of reserved EEPROM space for customer use. After the command code, the starting memory location must be entered followed by a block write, and terminated by the PEC number;

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1
Start location	A	Byte count	A

8	1	.....	8	1
first_byte	A	.....	Last - byte	A

8	1	1
PEC	A	P

To read contents from the EEPROM section

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

8	1	8	1
Memory location	A	Byte count ≤ 32	A

1	7	1	1
Sr	Slave address	Rd	A

8	1	.....	8	1
Byte 1	A	.....	Byte ≤ 32	A

8	1	1
PEC	No-ack	P

See footnotes on page 34

Test Function (0xDF)

Bit	Function	State
7	25ms stretch for factory use	1= stretch ON
5 - 6	reserved	
4	Or'ing test	1=ON, 0=OFF
2 - 3	reserved	
1	X	X
0	LED test	1=ON, 0=OFF

LEDS test ON: Will turn-ON simultaneously the front panel LEDs of the Rectifier sequentially 7 seconds ON and 2 seconds OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the rectifier being talked to and also to visually verify that the LEDs operate and driven properly by the micro controller.

LEDS test OFF: Will turn-OFF simultaneously the four front panel LEDs of the Rectifier.

OR'ing Test: This command verifies functioning of output OR'ing. At least two paralleled rectifiers are required. The host should verify that N+1 redundancy is established. If N+1 redundancy is not established the test can fail. Only one rectifier should be tested at a time.

Verifying test completion should be delayed for approximately 30 seconds to allow the rectifier sufficient time to properly execute the test.

Failure of the isolation test is not considered a rectifier FAULT because the N+1 redundancy requirement cannot be verified. The user must determine whether a true isolation fault indeed exists.

General performance descriptions

Default state: Rectifiers are programmed in the default state to automatically restart after a shutdown has occurred. The default state can be reconfigured by changing non-volatile memory (Store_user_code).

Delayed overcurrent shutdown during startup: Rectifiers are programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled front-ends during power up. If the overload persists beyond the 20 second delay, the front-end will revert back into its programmed state of overload protection.

Unit in Power Limit or in Current Limit: When output voltage is > $36V_{DC}$ the Output LED will continue blinking.

When output voltage is < $36V_{DC}$, if the unit is in the RESTART mode, it goes into hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

Restart after a latchoff: PMBus™ fault_response commands can be configured to direct the rectifier to remain latched off for over_voltage, over_temperature and over_current.

To restart after a latch off either of five restart mechanisms are available.

1. The hardware pin ON/OFF may be cycled OFF and then ON.
2. The unit may be commanded to restart via I2C through the Operation command by cycling the output OFF followed by ON.
3. Remove and reinsert the unit.
4. Turn OFF and then turn ON AC power to the unit.
5. Changing firmware from latch off to restart.

Each of these commands must keep the rectifier in the OFF state for at least 2 seconds, with the exception of changing to restart.

A successful restart shall clear all alarm registers, set the restarted successful bit of the Status_2 register.

A power system that is comprised of a number of rectifiers could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual rectifiers. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.

A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all rectifiers,
2. Toggling Off and then ON the ON/OFF (ENABLE) signal
3. Removing and reapplying input commercial power to the entire system.

The rectifiers should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual rectifiers.

See footnotes on page 34

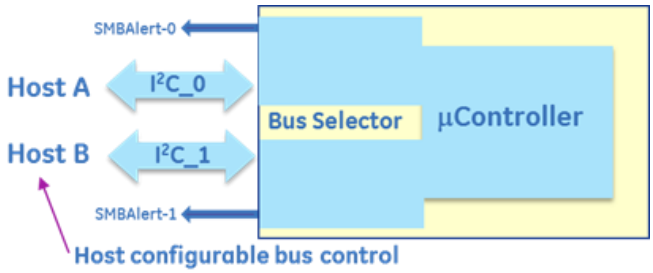
Auto_restart: Auto-restart is the default configuration for over-current and over-temperature shutdowns. These features are configured by the **PMBus™** fault_response commands

An overvoltage shutdown is followed by three attempted restarts, each restart delayed 1 second, within a 1 minute window. If within the 1 minute window three attempted restarts failed, the unit will latch OFF. If within the 1 minute less than 3 shutdowns occurred then the count for latch OFF resets and the 1 minute window starts all over again

Dual Master Control:

Two independent I²C lines and Alert# signals provide true communications redundancy allowing two independent controllers to sequentially control the rectifier.

A short or an open connection in one of the I²C lines does not affect communications capability on the other I²C line. Failure of a 'master' controller does not affect the rectifiers and the second 'master' can take over control at any time when the bus is idle.



Conceptual representation of the dual I2C bus system.

The Alert# line exciting the rectifier combines the Alert# functions of rectifier control and dual_bus_control.

Status_bus (0xD7): Bus_Status is a single byte read back. The command can be executed by either master at any time independent of who has control.

The µC may issue a clock stretch, as it can for any other instruction, if it requires a delay because it is busy with other activities.

Automatically resetting into the default state requires the removal of bias supply from the controllers.

Bit	Flag	Default
7	Bus 1 command error	0
6	Bus 1 SMBAlert enabled	0
5	Bus 1 requested control	0
4	Bus 1 has control of the PS	0
3	Bus 0 command error	0
2	Bus 0 SMBAlert enabled	0
1	Bus 0 requested control	0
0	Bus 0 has control of the PS	1

Command Execution: The master not in control can issue two commands on the bus, take_over_bus_control and clear_faults

Take_over_Bus_Control(0xD8): This command instructs the internal µC to switch command control over to the 'master' that initiated the request.

Actual transfer is controlled by the I²C selector section of the µC. A bus transfer only occurs during an idle state when the 'master' currently in control (in the execution process of a control command) has released the bus by issuing a STOP command. Control can be transferred at any time if the 'master' being released is executing a read instruction that does not affect the transfer of command control. Note; The µC can handle read instructions from both busses simultaneously.

The command follows PMBus™ standards and it is not executed until the trailing PEC is validated.

Status Notifications: Once control is transferred both SMBAlert lines should get asserted by the I²C selector section of the µC. The released 'master' is notified that a STATUS change occurred and he is no longer in control. The connected 'master' is notified that he is in control and he can issue commands to the rectifier. Each master must issue a clear_faults command to clear his SMBAlert signal.

If the SMBAlert signal was actually triggered by the rectifier and not the I²C selector section of the µC, then only the 'master' in control can clear the rectifier registers. Incomplete transmissions should not occur on either bus.

Fault Management

Certain transitionary states can occur before a final state is reached. The STATUS and ALARM registers will not be frozen into a notification state until the final

See footnotes on page 34

state is reached. Once a final state is reached the Alert# signal is set and the STATUS and ALARM registers will not get reinstated until a clear_faults is issued by the master. The only exception is that additional state changes may be added to the original list if further changes are noted.

All fault information is sticky. If the fault still persists after a clear_faults has been issued, then the fault state will reassert. All operational state information is not sticky.

The rectifier differentiates between **internal faults** that are within the rectifier and **external faults** that the rectifier protects itself from, such as overload or input voltage out of limits. The FAULT LED, FAULT PIN or i^2c alarm is not asserted for EXTERNAL FAULTS. Every attempt is made to annunciate External Faults. Some of these annunciations can be observed by looking at the input LEDs. These fault categorizations are predictive in nature. Therefore, there is a likelihood that a categorization may not have been made correctly.

State Change Definition

A state_change is an indication that an event has occurred that the MASTER should be aware of. The following events shall trigger a state_change;

- Initial power-up of the system when INPUT gets turned ON . This is the indication from the rectifier that it has been turned ON. Note that the master needs to read the status of each rectifier to reset the system_interrupt. If the rectifier is back-biased through the 8V_INT or the 5VSTB it will not issue an SMBALERT# when INPUT power is turned back ON.
- Whenever the rectifier gets hot-plugged into a working system. This is the indicator to the system (MASTER) that a new rectifier is on line.
- Any changes in the bit patterns of the STATUS and ALARM registers are a STATUS change which triggers the SMBALERT# flag. Note that a host-issued command such as CLEAR_FAULTS will not trigger an SMBALERT#

Hot plug procedures

Careful system control is recommended when hot plugging a rectifier into a live system. It takes about 15 seconds for a rectifier to configure its address on the bus based on the analog voltage levels present on the backplane. If communications are not stopped during this interval, multiple power supplies may respond to specific instructions because the address of the hot plugged rectifier always defaults to xxx0000 (depending on which device is being addressed within the rectifier) until the rectifier configures its address.

The recommended procedure for hot plug is the following: The system controller should be told which rectifier is to be removed. The controller turns the service LED ON, thus informing the installer that the identified rectifier can be removed from the system. The system controller should then poll the module_present signal to verify when the rectifier is re-inserted. It should time out for 15 seconds after this signal is verified. At the end of the time out all communications can resume.

Hot plug configuration

During hot plug the rectifier attempts to configure itself to the bus voltage of a working system. The following are the turn-ON steps implemented within the rectifier:

- Prior to turning ON the main output the rectifier reads the bus voltage present on the bus. If the bus voltage and the commanded voltage (either default or V_{margin}) are the same, the power supply proceeds to turn ON into its commanded value.
- If the bus voltage and the commanded voltage do not agree, the rectifier ignores the commanded voltage and waits for the external controller to command it to set its output voltage. This step is required to ensure that the plugged in rectifier does not attempt to source an entire system at an uncontrolled voltage level.
- If the bus voltage is below $40V_{dc}$ the rectifier proceeds to turn ON into its commanded value.

Failure Predictions

Alarm warnings that do not cause a shutdown are indicators of potential future failures of the rectifier. For example, if a thermal sensor failed, a warning is issued but an immediate shutdown of the rectifier is not warranted.

Another example of potential predictive failure mechanisms can be derived from information such as fan speed when multiple fans are used in the same

See footnotes on page 34

rectifier. If the speed of the fans varies by more than 20% from each other, this is an indication of an impending fan wear out.

The goal is to identify problems early before a protective shutdown would occur that would take the rectifier out of service.

Information only alarms: The following alarms are for information only, they do not cause a shutdown

- Over temperature warning
- V_{out} out-of-limits
- Output voltage lower than bus
- Unit in Power Limit
- Thermal sensor failed
- Or'ing (Isolation) test failure
- Power delivery
- Stby out of limits
- Communication errors

LEDs

Three LEDs are located on the front faceplate. The AC_OK LED provides visual indication of the INPUT signal function. When the LED is ON GREEN the rectifier input is within normal design limits.

The second LED is the DC_OK LED. When GREEN the DC output is present. When 'blinking' a power limit or overload condition exists. When OFF the output is not present.

The third LED is the FAULT LED. A continuous RED condition indicates that a fault exists and the rectifier has been shut down. Blinking of the RED LED in RS485 mode indicates that communications with the controller was not established. In I^2C mode, blinking of the FAULT LED indicates an OTW.

Remote upgrade

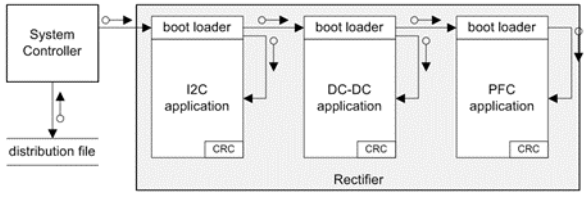
This section describes at a high-level the recommended re-programming process for the three internal micro controllers inside the rectifier when the re-programming is implemented in live, running, systems.

The process has been implemented in visual basic by OmniOn Critical Power for controller based systems positioned primarily for the telecommunications industry. OmniOn Critical Power will share its development with customers who are interested to deploy the re-programming capability into their own controllers.

For some customers internal system re-programming is either not feasible or not desired. These customers may obtain a re-programming kit from OmniOn Critical Power. This kit contains a turn-key package with the re-program firmware.

Conceptual Description: The rectifier contains three independent µControllers. The boost (PFC) section is controlled by the primary µController. The secondary DC-DC converter is controlled by the secondary µController, and I^2C communications are being handled by the I^2C Interface µController.

Each of the µControllers contains a boot loader section and an application section in memory. The purpose of the boot loader section is to facilitate the upgrading capability described here. All the commands for upgrading and memory space required for incrementally changing the application code are in this section. The application section contains the running code of the rectifier.



The system controller receives the upgrade package. It should first check whether an upgrade is required followed by upgrading those processors, one at a time, that are required to be upgraded. Each processor upgrade needs to be validated and once the upgrade is successfully completed the boot loader within each processor will permit the application to run after a reset. If the validation fails the boot loader will stay in its section. The system controller can attempt another upgrade session to see if it would complete successfully.

The Upgrade Package: This package contains the following files;

- **Manifest.txt –** The manifest describes the contents of the upgrade package and any incidental information that may be useful, for example, what this upgrade contains or why is this upgrade necessary

See footnotes on page 34

This file contains the version number and the compatibility code of the upgraded program for each of the three processors

- **Program.bin -** The upgraded program contents are located here. Each processor to be upgraded will have its own file.

Below is an example of an upgrade package

- Contents of the upgrade are in a zip file GP100H3R54TEZ.zip
- Unzipping the contents shows the following files
  GP100H3R54TEZ.pfc.bin
  GP100H3R54TEZ.sec.bin
  manifest.txt
- Opening manifest.txt shows the following
  # Upgrade manifest file
  # Targets: GP100H3R54TEZ PFC and SEC
  # Date: Tue 01/14/2014 14:25:09.37
  # Notes:
- Program contents
  >p,GP100H3R54TE_P01,GP100H3R54TEZ_PFC.bin,1.18
  >s,GP100H3R54TE_S01,GP100H3R54TEZ_SEC.bin,1.1

  compatibility code, new program, revision number

Upgrade Status Indication: The FAULT LED is utilized for indicating the status of the re-programming process.

Status	Fault LED	Description
Idle	OFF	Normal state
In boot block	Wink	Application is good
Upgrading	Fast blink	Application is erased or programming in progress
Fault	ON	Erase or re-program failed

Wink: 0.25 seconds ON, 0.75 seconds OFF

Fast Blink: 0.25 seconds ON. 0.25 seconds OFF

Upgrade procedure

1. Initialization: To execute the re-programming/ upgrade in the system, the module to be re-programmed must first be taken OFF-line prior to executing the upgrade. If the module is not taken OFF-line by the system controller, the boot loader will turn OFF the output prior to continuing with the re-programming operation. Note: Make sure that sufficient power is provided by the remaining on-line power supplies so that system functionality is not jeopardized.

2. Unzip the distribution file

3. Unlock upgrade execution protection by issuing the command below;

Password(0xE0): This command unlocks the upgrade commands feature of the module by sending the characters 'UPGD'.

1	8	1	8	1	8		1
S	Slave addr	Wr	A	Cmd – 0xE0	A	Byte count - 4		A

8	1	.....	8	1	8	1	1
Byte 0 - U	A		Byte 4 - D	A	PEC	A	P

4. Obtain a list of upgradable processors (optional)

Target list(0xE1) : This command returns the upgradable processors within the module. The byte word is the ASCII character of the processor (p, s, and i). The command is optional to the user for information only.

1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE1	A

1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count - n	A

8	1	.....	8	1	8	1	1
Byte 0	A		Byte n	A	PEC	No-Ack	P

Potential target processors are the following:

p – primary (PFC)
s – secondary (DC-DC)
i – I²C

5. Verify upgrade compatibility by matching the upgrade compatibility code in the manifest.txt file to the module compatibility code of the target processor.

Compatibility code (0xE2): The compatibility code consists of up to 16 characters defining the hardware configuration. To read the compatibility codes of each processor in the module execute the following read:

1	8	1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE2	A	Target-x	A

1	8	1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 16	A	Byte 0	A

.....	8	1	8	1	1
	Byte 15	A	PEC	No-Ack	P

Where Target-x is an ASCII character pointing to the processor to be updated;

p – primary (PFC)
s – secondary (DC-DC)
i – I²C

See footnotes on page 34

6. Check the software revision of the target processor and compare it to the revision in the upgrade. If the revisions are the same, or the module has a higher revision then no upgrade is required for the target processor.

Software revision(0xE3): This command returns the software revision of the target.

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE3	A	Target-x	A

1	8		1	8	1
Sr	Slave addr	Rd	A	Major revision	A

8	1	8	1	1
Minor revision	A	PEC	No-Ack	P

7. Verify the capability of each processor

Memory capability (0xE4): Provides the specifics of the capability of the device to be reprogrammed

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE2	A	Target-x	A

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Byte count = 7	A	Max bytes	A

8	1	8	1	8	1	8	1
ET-LS B	A	ET-MSB	A	BT-LSB	A	BT-MSB	A

8	1	8	1	8	1	1
App_CRC_LSB	A	App_CRC_MSB	A	PEC	No-Ack	P

Where the fields definition are shown as below:

Max Bytes	Maximum number of bytes in a data packet
ET	Erase time for entire application space (in mS)
BT	Data packet write execution time (uS)
APP_CRC	Returns the application CRC-16 calculation. If the calculation returns invalid, the reprogram failed. (See application status(0xE5) command)

This information should be used by the host processor to determine the max data packet size and add appropriate delays between commands.

8. Verify availability: The Application status command is used to verify the present state of the boot loader.

Application status (0xE5): Returns the Boot Loader's present status

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE5	A	Target-x	A

1	8		1	8	1	8	1	1
Sr	Slave addr	Rd	A	Status	A	PEC	No-Ack	P

Status bits:

0x00 Processor is available 0x01 Application erased 0x02 CRC-16 invalid 0x04 Sequence out of order 0x08 Address out of range	0x10 Reserved 0x20 Reserved 0x40 Manages downstream µC 0x80 In boot loader

Status of the application should be checked after the execution of successive commands to verify that the commands have been properly executed.

9. Issue a Boot Loader command with the enter boot block instruction

Boot loader (0xE6): This command manages the upgrade process starting with entering the sector, erasing the present application, indicating completion of the upload and finally exiting from the boot sector, thereby turning over control to the uploaded application.

1	7	7	7	8	1	8	1
S	Slave addr	Wr	A	Cmd – 0xE6	A	Target-x	A

8	1	8	1	1
Data	A	PEC	A	P

Data:

1=enter boot block (software reboot)

2=erase

3=done

4=exit[23] boot block (watchdog reboot)

Note: The target µC field is ignored for enter and exit commands. During this process if the output of the module was not turned OFF the boot loader will turn OFF the output

See footnotes on page 34

10. Erase and program each µC using the Boot Loader command, starting with the PFC.
11. Wait at least 1 second after issuing en erase command to allow the µC to complete its task.
12. Use command 0xE5 to verify that the PFC µC is erased. The returned status byte should be 0x81.
13. Use the Data Transfer command to update the application of the target µC.

Data transfer (0xE7): The process starts with uploading data packets with the first sequence number (0x0000).

1	8		1	8	1	8	1
S	Slave addr	Wr	A	Cmd - 0xE7	A	Target-x	A

8	1	8	1	8	1
Seq-LSB	A	Seq-MSB	A	Byte Count = n	A

8	1		8	1	8	1	1
Byte 0	A	.....	Byte n-1	A	PEC	A	P

After completion of the first data packet upload the Boot loader increments the sequence number. A subsequent read to the boot loader will return the incremented sequence number and a STATUS byte. This is a validity check to ensure that the sequence number is properly kept. The returned STATUS byte is the same as the application status response. It is appended here automatically to save the execution of another command. It should be checked to ensure that no errors are flagged by the boot loader during the download. If an error occurred, terminate the download load and attempt to reprogram again.

1	8		1	8	1
S	Slave addr	Wr	A	Cmd - 0xE4	A

1	8		1	8	1
Sr	Slave addr	Rd	A	Byte count = 3	A

1	8	8	1	8	1	8	1	1
Seq-LSB	A	Seq-MSB	A	Sta-tus	A	PEC	No-Ack	P

Sequence number validation takes place after each data block transfer. The next data block transfer starts with the sequence number received from the boot loader.

The host keeps track of the upload and knows when the upload is completed.

14. Execute a Boot loader command to tell the PFC µC that the transfer is done.

    At the completion signal, the PFC µC should calculate the PEC value of the entire application. The last two bytes of the loaded application were the CRC-16 based PEC calculation.

    Wait for at least 1 second to allow time for the PFC µC to calculate the error checking value.
15. Execute an Application status command to verify that the error check is valid. The returned status should be 0x80.
16. Execute a Boot loader command to exit boot block. Upon receipt of the command the PFC µC will transfer to the uploaded application code.
17. Wait for at least 1 second.
18. Use command 0xE1 to verify that the PFC µC is now in the application code. The returned status data bte should be 0x00.
19. Repeat the program upgrade for the Secondary and I^2C µC's, if included in the upgrade package.

Product Ordering Code

Although the Ordering Code number is not required for the upgrade process in its present form, it may be useful when upgrading multiple version of the same product in order to differentiate product upgrade requirements.

Product Ordering Code (0xE8):

1	8		1	8	1
S	Slave addr	Wr	A	Cmd - 0xE8	A

1	8		1	8	1
Sr	Slave addr	Rd	A	Byte count = 11	A

8	1	.....	8	1	8	1	1
Byte 0	A		Byte 10	A	PEC	No-Ack	P

Error handling: The Boot loader will not start the application if errors occurred during the re-program stage. The controlling program could restart the upgrade process or terminate the upgrade and remove the offending module from service.

See footnotes on page 34

Black box

Contents of the black box and more detailed information about the specifics of the feature are described in a separate document. The intent here is to provide a high level summary This feature includes the following;

1. A rolling event Recorder
2. Operational Use Statistics

The rolling event recorder

The purpose of the black box is to provide operational statistics as well as fault retention for diagnostics following either recoverable or non-recoverable fault events. Sufficient memory exists to store up to 5 time-stamped snapshot records (pages) that include the state of the status and alarm registers and numerous internal measurement points within the power supply. Each record is stored into nonvolatile memory at the time when a black box trigger event occurs. Once five records are stored, additional records over-write the oldest record.

The memory locations will be cleared, when the product is shipped from the OmniOn factory.

Operational use statistics

This feature of the black box includes information on the repetition and duration of certain events in order to understand the long-term operational state of the power supply. The events are placed into defined buckets for further analysis. For example; the power supply records how long was the output current provided in certain load ranges.

Accessing the event records

The event records are accessed by uploading the entire contents of the black box of the power supply into a folder assigned by the user. Within the I^2C protocol this upload is accomplished by the upload_black_box (0xF0) command described below. OmniOn provides a Graphical User Interface (GUI) that de-codes the contents of the black box into a set of records that can be reviewed by the user.

Upload black box(0xF0): This command executes the upload from the power supply to a file of the user's choice.

The 100ms delay prior to the restart is mandatory to provide enough time for the power supply to gather the required data from the secondary DSP controller.

1	8		1	8	1
S	Slave addr	W r	A	Cmd – 0xF0	A

8	1	8	1
Start address - msb	A	Start address - lsb	A

8	1
Length = N (≤ 32)	A

..... delay 100ms

1	8		1	8	1	8	1
Sr	Slave addr	Rd	A	Length ≤ 32	A	Byte 0	A

.....

8	1	8	1	1
Byte N-1	A	PEC	No-Ack	P

If a transmission error occurs, or if the uC did not receive the data from the DSP, the uC may set the length to 0, issue a PEC and terminate the transmission.

The data array supported by rev 1.3 of the OmniOn Interface Adapter is 32 x 64 comprising 2048 bytes of data.

Start Address	0 ..... Byte 31
0000h	
0020h	
0040h	
.	
.	
.	
.	
.	
.	
.	
07E0h	

See footnotes on page 34

Appendix

Bus transfer reporting

The events below concentrate on what happens when a clear_faults is issued. The systemcontroller neds to be intelligent enough to inquire the status of the power supply before issuing a clear_faults. Otherwise, it would lose whatever information may be in the status registers.

	Operation	Alert#1	Alert#0	Status_bus	Status_word	Status_cml	
1	i²c1 - command sent, not in control	1	0	0xC1	0x0000	0x00	
2	i²c1 issues a clear_faults	0	0	0x01	0x0000	0x00	
3	i²c0 in control, unit issues a fault	1	1	0x01	event1	0x00	
4	i²c1 takes over control	1	1	0x74	event1	0x00	
5	i²c1 read system status	1	1	0x74	event1	0x00	Controller needs to read status before clearing the registers
6	i2c1 issues a clear_fault	0	1	0x14	0x0000	0x00	Assuming that the event has cleared
7	i²c0 read system status	0	1	0x14	0x0000	0x00	The Alert remains because of status_bus, not because of unit fault
8	i²c0 issues a clear fault	0	0	0x10	0x0000	0x00	
9	i²c0 in control, unit issues a fault	1	1	0x01	event1	0x00	
10	i²c1 issues clear fault	0	0	0x01	0x0000	0x00	Assuming that the event has cleared
11	i²c1 in control	0	0	0x10	0x0000	0x00	
12	i²c0 takes over control	1	1	0x47	0x0000	0x00	
13	i²c0 issues a clear_fault	1	0	0x41	0x0000	0x00	
14	i²c1 issues a clear_fault	0	0	0x01	0x0000	0x00	
15	i²c1 in control	0	0	0x10	0x0000	0x00	
16	i²c0 issues a command	0	1	0x1C	0x0000	0x00	The command is rejected because i²c0 is not in control
17	i²c0 issues a clear_fault	0	0	0x10	0x0000	0x00	
18	i²c1 issues a bad command	1	0	0x10	0x0002	0x80	
19	i²c1 issues a clear_fault	0	0	0x10	0x0000	0x00	

Rules:

Side in control is the only one that can clear the status registers.
The side in control can not clear the alert of the side not in control
A power supply alarm should not set the status_bus registers.

See footnotes on page 34

Table 2: Alarm and LED state summary

	Rectifier LED State				Monitoring Signals		
Condition	AC OK Green	DC OK Green	Fault Red		Fault	PFW	Module Present
OK	1	1	0		HI	HI	LO
Thermal Alarm (5°C before shutdown)	1	1	Blinks		HI	HI	LO
Thermal Shutdown	1	0	1		LO	LO	LO
Defective Fan[2,4]	1	0	1		LO	LO	LO
Blown AC Fuse in Unit	1	0	1		LO	LO	LO
AC Present but not within limits	Blinks	0	0		HI	HI	LO
AC not present[1]	0	0	0		HI	LO	LO
Boost Stage Failure	1	0	1		LO	LO	LO
Over Voltage Latched Shutdown	1	0	1		LO	LO	LO
Over Current[5]	1	Blinks	0		HI	Pulsing[4]	LO
Non-catastrophic Internal Failure[2]	1	1	1		LO	HI	LO
Missing Module							HI
Standby (remote)	1	0	0		HI	LO	LO

[1] This signal is correct if the power supply is back biased from other power supplies in the shelf .

[2] Any detectable fault condition that does not cause a shutting down. For example, ORing FET failure, boost section out of regulation, etc.

[3] Signal transition from HI to LO is output load dependent

[4] Pulsing at a duty cycle of 1ms as long as the unit is in overload.

[5] "DC OK" blinks &" Fault" off occurred when PSU output current close to the OCP limit slowly, and the output voltage drop to -5%Vo. If a heavy load added suddenly, will get another indication:" DC OK" off &" Fault" LED on.

Table 3: Signal Definitions

Signals (Fault, PFW, OTW, Power Capacity) are open drain FETs. An active LO signal (< 0.4V_{DC}) state. Signals are referenced to Logic_GRD unless otherwise stated.

Function	Label	Type	Description
Remote ON/OFF	ON/OFF	Input	**I²C mode:** When shorted to Logic_GRD turns ON the main output
Output voltage adjust	V_{prog}	Input	Changes the output voltage (see table). Ref: Logic_GND
Power good warning	PFW	Output	**I²C mode:** Open drain FET; normally HI, Changes to LO when output is lower than limit Ref: Logic_GND
Internal failure	Fault	Output	**I²C mode:** An open drain FET; normally HI, changes to LO when internal failure occurred Ref: Logic_GND
Module Present	MOD_PRES	Output	Short pin, Connected to Logic_GRD notifies the system that module is present. Ref: Logic_GND
Defines communications	Protocol	Input	**I²C mode:** no-connect. **RS485 mode:** 1k - 5kΩ resistor connected to Vout (-).
Slot Address/Interlock	Slot_ID INTERLOCK	Input	Short pin referenced to Vout(-) . This signal provides the last-to-make and first-to-break function to properly control the rectifier for hot plug and hot disengagement. **RS485 mode:** A voltage level identifies the rectifier slot address in a shelf. **I²c mode:** Connected to Vout (-).

See footnotes on page 34

Table 3: Signal Definitions (continued)

Function	Label	Type	Description
Unit Address	Unit_ID	Input	**I²C mode:** A resistor to Logic_GRD (see definition in spec)
Rack Address	Rack_ID	Input	**I²C mode:** An external resistor divider from 5VA to Logic_GRD (see definition in spec).
DC-DC Back bias	8V_INT	Bi-direct	Used to back bias the DSP from other operating Power supplies. Ref: V_{out} (-). Connect each unit 8V_int together in units main output is in parallel.
Standby power	5VA	Output	5V @ 0.75A provided for external use. This output is always ON and or'ed isolated. Connect each unit 5VA together in units main output is in parallel. Ref: LGND
Current Share	Ishare	Bi-direct	A single wire active-current-share interconnect between modules Ref: V_{out} (-). Connect current share together when units main output are in parallel.
I²C Line 0, I²C Line 1	SCL_0, SCL_1	Input	Clock signal pins of the two redundant buses. No internal pull ups are present. Ref: LGND
I²C Line 0, I²C Line 1	SDA_0, SDA_1	Bi-direct	Data signal pins of the two redundant buses. No internal pull ups are present. Ref: LGND
SMBALERT# Line 0, Line 1	ALERT#_0, ALERT#_1	Output	Interrupt signal pins of the two redundant buses. No internal pull ups are present Active LO. Ref: LGND

FOOTNOTES

* UL is a registered trademark of Underwriters Laboratories, Inc.

† CSA is a registered trademark of Canadian Standards Association.

‡ VDE is a trademark of Verband Deutscher Elektrotechniker e.V.

§ This product is intended for integration into end-user equipment. All CE marking procedures of end-user equipment should be followed. (The CE mark is placed on selected products.)

** ISO is a registered trademark of the International Organization of Standards

+ The PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF)

[1] See the derating guidelines under the Environmental Specifications section

[2] It may be necessary that a label, bearing the following warning, or similar wording, be affixed adjacent to the end equipment primary power connection: HIGH LEAKAGE CURRENT Earth connection essential before connecting supply

[3] Below -5°C, the rise time is approximately 5 minutes to protect the bulk capacitors.

[4] Remote on/off is shorted to logic_gnd before AC input applied

[5] AC input already applied and completed internal soft-start.

[7] Overload retries must incorporate normal soft-start turn-ON.

[8] Actual OVP point may beyond setting point due to delay, but will be lower than 65V.

[9] default setting can be changed through PMBUS command by user, and stored into non-volatile memory.

[10] V_{stdby} is generally 3.3V or 5V

[11] Clock, Data, and SMBAlert need to be pulled up to VDD externally.

[12] Above 2.5A of load current

[13] Temperature accuracy reduces non-linearly with decreasing temperature

[14] Designed to start and work at an ambient as low as -40°C, but may not meet operational limits until above -5°C

[15] The maximum operational ambient is reduced in Europe in order to meet certain power cord maximum ratings of 70°C. The maximum operational ambient where 70°C rated power cords are utilized is reduced to 60°C until testing demonstrates that a higher level is acceptable. At high input voltage ($530V_{AC}$), the maximum temperature rating is reduced to 70°C.

[16] test in OmniOn standard shelf

[17] Criteria A at $480V_{ac}$ input, Criteria B at $380V_{ac}$ input

[18] Criteria A at $480V_{ac}$ input, Criteria B at $380V_{ac}$ input

[19] Refer ride through spec

[20] Accuracy ± 5% (+5V accuracy ± 4%)

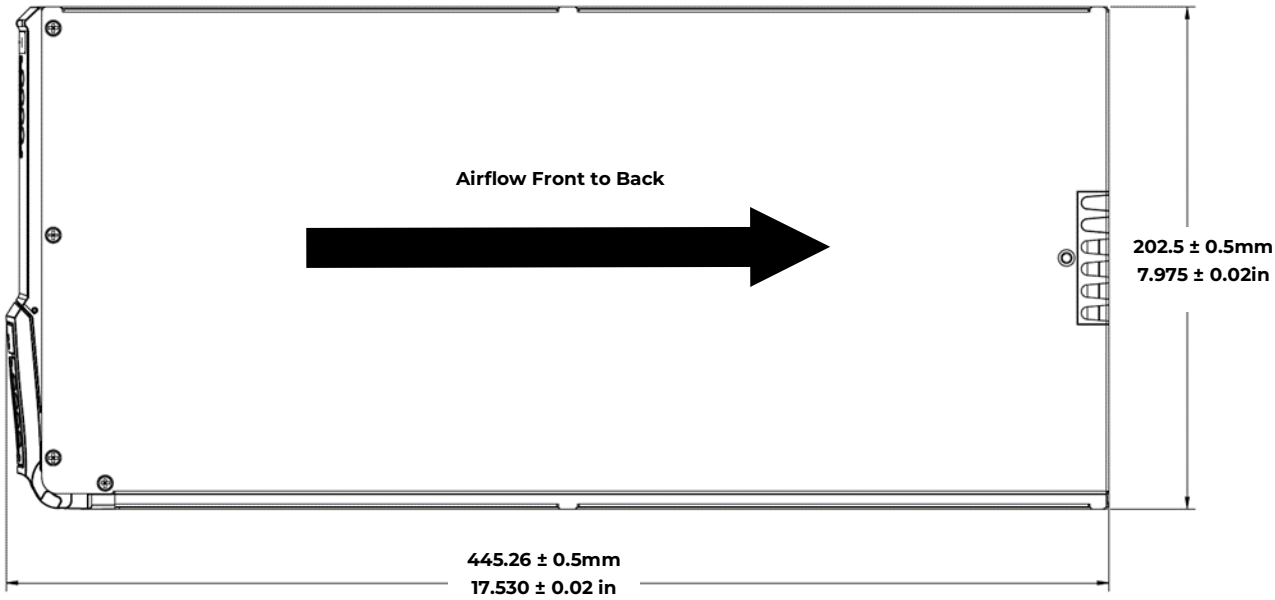
[21] Only latched (0x80) or restart (0xC0) are supported

[22] Only latched (0x80) or restart (0xC0) are supported

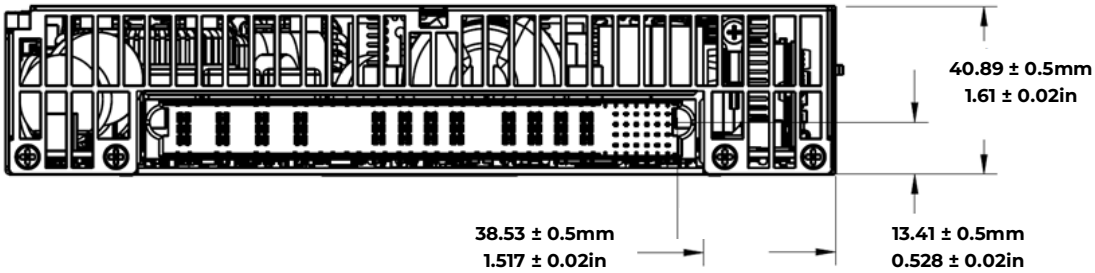
[23] The 'exit boot block' command is only successful if all applications are valid, otherwise, control remains in the boot block

[24] A fan failure would cause shutdown of the output only if it would trigger a thermal event.

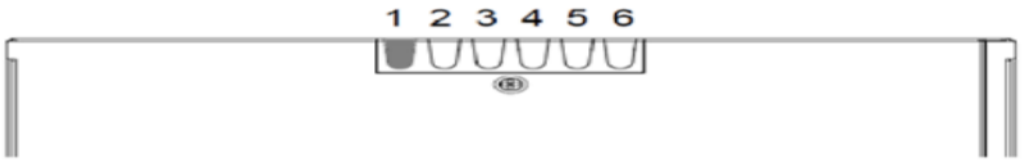
Mechanical Outline



Top View **[Note: add safety label to side of unit per UL, EC directives, TUV, Power Systems Practices]**



Rear View



Keying

Product	Keying Location Knotched
I²C communications	1

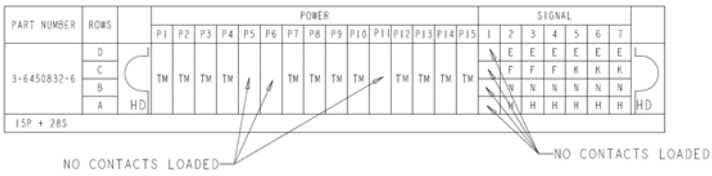
Front View: Faceplate Color: Spattered Finish CO White (OS11148)

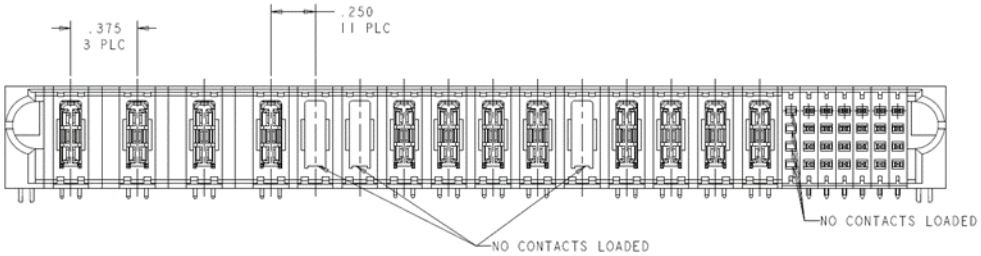
Front Panel LEDs

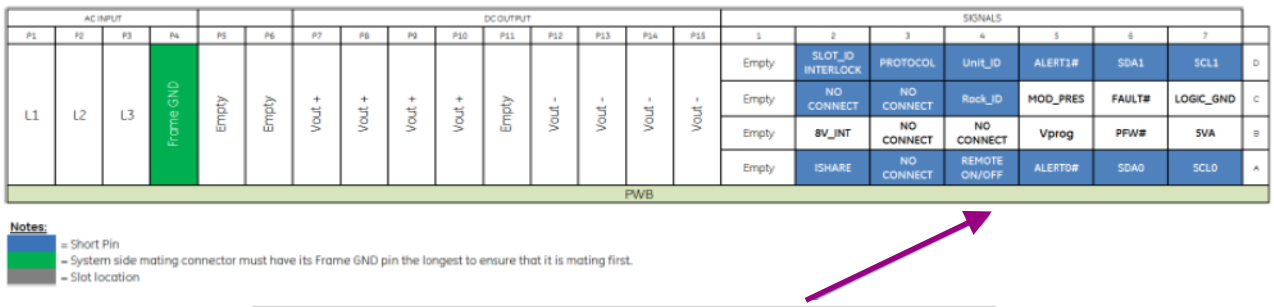
Symbol	Color	Function
☐~		**ON:** Input ok **Blinking:** Input out of limits
☐ !		**ON:** Fault **Blinking:** RS485 – loss of communications I²C - Impending failure warning
☐ ⎓		**ON:** Output ok **Blinking:** Overload

Mating Connector

Power supply side: Tyco 3-6450832-6







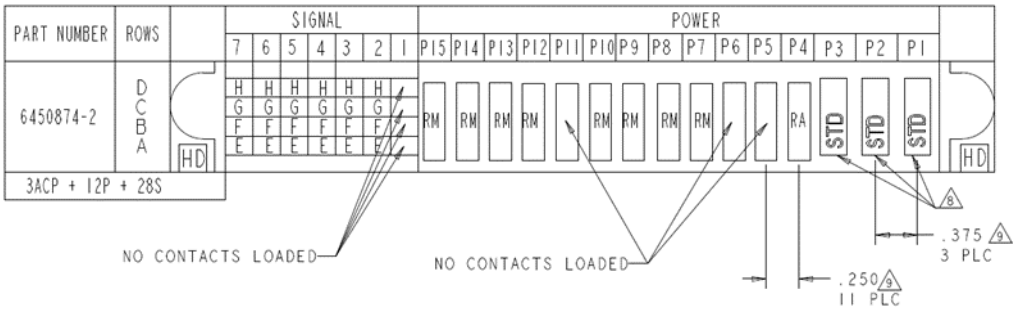
Notes:
= Short Pin
= System side mating connector must have its Frame GND pin the longest to ensure that it is mating first.
= Slot location

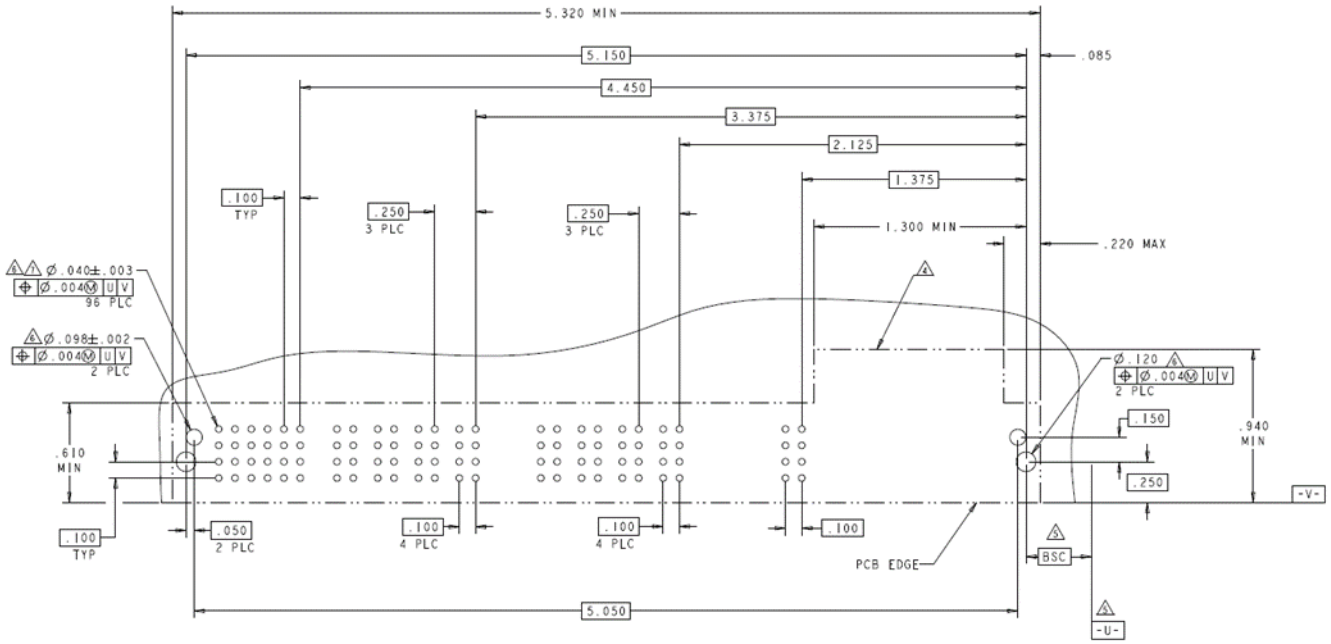
SIGNALS							
1	2	3	4	5	6	7	
Empty	SLOT_ID INTERLOCK	PROTOCOL	Unit_ID	ALERT1#	SDA1	SCL1	D
Empty	NO CONNECT	NO CONNECT	Rack_ID	MOD_PRES	FAULT#	LOGIC_GND	C
Empty	8V_INT	NO CONNECT	NO CONNECT	Vprog	PFW#	5VA	B
Empty	ISHARE	NO CONNECT	REMOTE ON/OFF	ALERT0#	SDA0	SCL0	A

Technical Specifications (continued)

System side connector: Tyco soldered version: 6450874-2

press-fit version: 6450884-2





Recommended PCB Layout

Ordering Information

Please contact your OmniOn Sales Representative for pricing, availability and optional features.

Item	Description	Comcode
GP100H3M50TEZ-FB	110A rectifier with isolated dual I²C communications, 18V~58V, RoHS 6/6, Conformal Coated	1600127198A

Accessories

Item	Description	Comcode
Pigtail assembly kits 	Single-unit cable assembly that mates with rectifier Blind-Mate connector. (sold as a component; equipment containing this harness requires safety certification)	1600206859A
Dongle	Isolated Interface Adapter Kit – interface between a USB port and the I2C connector on the rectifier interface board.	150036482
Remote upgrade	This GUI upgrades the application codes of all three processors inside the power supply. Available in both I²C and GP modes of operation. Requires both the interface board and the Isolated Interface Adapter kit revision 1.5 or higher. **omnionpower.com**	Free download
Software: OmniOn Digital Power Insight™	Graphic user interface with I2C communication.	

Contact Us

For more information, call us at

1-877-546-3243 (US)

1-972-244-9288 (Int'l)

Change History (excludes grammar & clarifications)

Revision	Date	Description of the change
1.2	12-31-2021	Updated as per template
1.3	11-21-2023	Updated as per OmniOn template

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