DATASHEET

FPLX015A0XY3-SRZ Non-Isolated DC-DC Power Module

6 V_{DC} - 14 V_{DC} input; 0.45 V_{DC} to 3.6 V_{DC} output; 15 A Output Current

RoHS Compliant



The OmniOn Power™ FPLX015A0XY3-SRZ Digital DLynx III™ power module is a non-isolated dc-dc converter that can deliver up to 30 A of output current. It operates over a wide input voltage range from 6.0 V_{DC} to 14 V_{DC} and provides precisely regulated output voltage programmable from 0.45 V_{DC} to 3.6 V_{DC} via pin strap resistor or PMBus™.

The module employs fast Constant On Time (COT) control scheme that is stable with ceramic output capacitors without external compensation, simplifies design efforts and achieves fast transient response.

Other main features include optional diode emulation mode for improved light load efficiency, monotonic start-up with selectable soft-start time, pre-bias start-up, digital PMBus interface, programmable enable logic and control, input over-voltage protection, output under-voltage and over-voltage protections, over-temperature protections and more. The module supports an extensive set of PMBus commands for control and monitoring of system parameters. The FPLX015A0XY3-SRZ power module is highly configurable, and yet easy to use.

Applications

- Telecommunications and networking equipment
- Broadband and communications equipment
- Servers, storage and computing applications
- Test and Measurement equipment
- Industrial and medical equipment
- DSP, FPGA, ASIC, CPU and networking processor applications
- Programmable logic applications
- Distributed bus power architectures and mixed voltage systems
- ATCA cards, Compact PCI / PCI Express / PXI Express applications

Features

- Compliant to RoHS II EU Directive 2011/65/EC and amended Directive (EU) 2015/863
- Compliant to IPC-9592 (Sept. 2008), Category 2, Class 2
- Compliant to REACH Directive (EC) No 1907/2006
- Compatible with a Pb-free or SnPn reflow soldering process
- Wide Input voltage range: 6.0 V_{DC} – 14 V_{DC}
- Output voltage programable from 0.45 V_{DC} to 3.6 V via PMBus or external pinstrap resistor
- Delivers up to 15 A output current
- Supports Voltage Rails requiring 3% transient tolerance
- Constant On Time control scheme provides fast transient response and stability without external compensation.
- Tightly regulated output voltage
- Low output ripple and noise
- Small size: 10 mm x 10 mm x 9.4 mm
  0.394 in x 0.394 in x 0.37 in
- Digital interface compliant to PMBus Rev.1.3 protocol
- Programmable enable logic with On/Off Control.
- Protections: OVP, UVP, OCP, OTP
- Wide operating temperature range -40°C to 85°C.
- Excellent Thermal Performance – Module delivers full output @ 12V_{IN}, 1V_{OUT}, 85°C ambient temperature without any forced airflow (NC—natural convection).
- UL* 62368-1, 3rd Ed. Recognized, and VDE (EN62368-1 3rd Ed.) Licensed.
- ISO** 9001 and ISO14001 certified manufacturing facilities.

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Quick start

Quick Start process for

- **External Enable**
- **Vout setting through PMBus, ignoring strap**
- **Change Enable Option to PMBus**

1. Keep EN pulled High to keep Output OFF.
2. Power up module
3. Switch VBT control into PMBus control by setting following register value
   VBOOT_OVERRIDE_PIN as 1
   FOVP_OVERRIDE_PIN as 1
   ROVP_OVERRIDE_PIN as 1
   VOUT_MAX as 2.25 V
4. Configure required output voltage through VOUT_COMMAND (0X21)
5. Set POWER_GOOD_ON as 0.359V or 93% of VOUT
6. Set POWER_GOOD_OFF as 0.359V or 80% of VOUT
7. Set VOUT_OV_FAULT_LIMIT as 2.2V or less (such as required VOUT_COMMAND—200mV)
8. Set VOUT_UV_FAULT_LIMIT as 0.3 or higher (such as required VOUT_COMMAND –200mV)
9. Set VOUT_UV_FAULT_LIMIT as 0.3V
10. If module has to be turned on using ON/OFF command use ON_OFF_CONFIG (0x02) to change setting
11. Remember to check VOUT_SCALE_LOOP value based on resistor used. The value is 0xE808 for 0.45 - 2.0 V output voltages.
12. If changes are final and configuration can be stored in NVM with STORE_USER_ALL (0x15).
13. Pull EN low to turn on module output

Quick Start process for

- **External Enable**
- **External VBT Pinstrap resistor**

1. Keep EN pulled high to make output off
2. Power up module
3. Check VBT pin is connected to required resistor according to the table for VOUT setting from VBT pin (page 13). Never leave VBT as floating.
4. Pull EN low to turn on module output

NOTE: In VBT+PMBus mode, the boot-up voltage is determined by an external strapping resistor between the VBT pin and ground, VOUT_MAX/MIN, POWER_GOOD_ON/OFF ,and VOUT_OV/UV_FAULT_LIMIT values are automatically adjusted based on the VBT resistor value. After power-on, users can still modify these register values via PMBus. However, these changes will be overridden by the VBT resistor configuration during the next power cycle—even if they are programmed into non-volatile memory (NVM).

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Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Operational functionality of the device is not implied at these or any other conditions in the excess of those given in the operations sections of the data sheet. Exposure to the absolute maximum ratings for extended periods may adversely affect the device reliability.

Parameter	Symbol	Min	Max	Unit
Input Voltage (continuous)	V_{IN}	-0.3	14.5	V
Operating Ambient Temperature	T_A	-40	85	°C
Storage Temperature		-55	125	°C

CAUTION: This power module is not internally fused. An input line fuse must always be used.

This power module can be used in a wide variety of applications, ranging from simple standalone operation to an integrated part of sophisticated power architecture. To preserve maximum flexibility, internal fusing is not included. However, to achieve maximum safety and system protection, always use an input line fuse. The safety agencies require a fast-acting fuse with a maximum rating of 30 A, 100 V (see Safety Considerations section). Based on the information provided in this Data Sheet on inrush energy and maximum dc input current, the same type of fuse with a lower rating can be used. Refer to the fuse manufacturer's Data Sheet for further information.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
PGOOD, PROG, VBT, VOSENP, SM_DATA, SM_CLK, SM_ALERT		0	3.6	V
VOSENM		- 0.3	0.3	V
EN		0	25	V

Electrical Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	All	V_{IN}	6.0		14.0	V_{DC}
Maximum Input Current (V_{IN}=6.0V to 14V, I_O=$I_{O,max}$)	All	$I_{IN,max}$			10	A_{DC}
Input No Load Current (V_{IN} = 12V_{DC}, I_O = 0, module enabled)	$V_{O,set}$ = 0.45V_{DC}	$I_{IN,No\ load}$	45	47	53	mA
	$V_{O,set}$ = 0.7V_{DC}	$I_{IN,No\ load}$	50	54	60	mA
	$V_{O,set}$ = 2.0V_{DC}	$I_{IN,No\ load}$	57	63	76	mA
	$V_{O,set}$ = 3.0V_{DC}	$I_{IN,No\ load}$	85	101	135	mA
	$V_{O,set}$ = 3.6V_{DC}	$I_{IN,No\ load}$	145	155	216	mA
Input Stand-by Current (V_{IN} = 12V_{DC}, module disabled)	All	$I_{IN,stand-by}$	10	11	12	mA
Inrush Transient	All	I^2t			1.8	A^2s
Input Reflected Ripple Current, peak-to-peak (5Hz to 20MHz, 1µH source impedance; V_{IN} =6 to 14 V, I_O= I_{Omax})	All		56	70	85	mA_{p-p}
Input Ripple Rejection (120Hz)	All			-83		dB
Output Voltage Set-point accuracy						
-40°C to 85°c, V_O=0.45 to 2.0 V (without divider)	All	0.45 - 2.0		0.5		$\%V_{O,SET}$
-40°C to 85°c, V_O=2.0 to 3.6V (with divider)	All	2.0 - 3.6		0.5		$\%V_{O,SET}$

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Electrical Specifications (continued)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
PMBus Adjustable Output Voltage Range	All	V_O	0.45		3.6	V_{DC}
PMBus Output Voltage Adjustment Step Size	All			0.244		mV
Remote Sense Range	All		0		2.56	V_{DC}
Output Ripple and Noise on nominal output 1.0V (V_{IN}=$V_{IN,\ nom}$ and I_O=$I_{O,\ min}$ to $I_{O,\ max}$ C_O = 2x470µF || 20x47 µf ceramic capacitors)						
Peak-to-Peak (5Hz to 20MHz bandwidth)		I_O		6		mV_{pk-pk}
RMS (5Hz to 20MHz bandwidth)		I_O		2		mV_{RMS}
External Capacitance Minimum and maximum C_{OUT} tested shown in table For stability one capacitor with ESR >10mΩ is required. Additional capacitance could be used using simulation and test board	All	$C_{O,\ TYPICAL}$	962	6060	Per Simulation from Power Module Wizard for output voltages <=1V	µF
Derated Output Current V_{IN}= 12V_{DC}, $T_{AMBIENT}$=84°C Natural Convection (NC)	All	$I_{o,\ lim}$		15		A_{DC}
V_{IN}= 12V_{DC}, $T_{AMBIENT}$=85°C 50 lfm	All	$I_{o,\ lim}$		15		A_{DC}
V_{IN}= 12V_{DC}, $T_{AMBIENT}$=85°C Natural Convection (NC)	$V_{O,set}$ ≤ 3.4V_{DC}	$I_{o,\ lim}$		15		A_{DC}
Efficiency	$V_{O,set}$ = 0.45V_{DC}			82		%
V_{IN}= 12V_{DC}, T_A=25°C	$V_{O,\ set}$ = 0.7V_{DC}			86		%
I_O=$I_{O,\ max}$, V_O= $V_{O,set}$	$V_{O,\ set}$ = 1.0V_{DC}	η		89		%
	$V_{O,set}$ = 2.0V_{DC}			92		%
	$V_{O,set}$ = 3.6V_{DC}			94		%
Switching Frequency (steady state)	All	f_{sw}		800		kHz
Dynamic Load Response (VIN= 12Vdc, TA=25°C, V_O=2.0 to 3.6V, step 25-75-25% $I_{O,MAX}$ at 10A/us)						
Maximum deviation from setpoint	All				1	$\%V_{O,SET}$
Settling time (to within 10% of ($V_{O,PK}$ – $V_{O,SET}$)	All				4	µs
Dynamic Load Response (VIN= 12Vdc, TA=25°C, V_O=0.7 to 2.0V, step 25-75-25% $I_{O,MAX}$ at 10A/us)						
Maximum deviation from setpoint	All				2.5	$\%V_{O,SET}$
Settling time (to within 10% of ($V_{O,PK}$ – $V_{O,SET}$)	All				5	µs
Dynamic Load Response (VIN= 12Vdc, TA=25°C, V_O=0.45 to 0.7V, step 25-75-25% $I_{O,MAX}$ at 10A/us)						
Maximum deviation from setpoint	All				4	$\%V_{O,SET}$
Settling time (to within 10% of ($V_{O,PK}$ – $V_{O,SET}$)	All				25	µs

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Feature Specifications

Parameter	Condition	Symbol	Min	Typ	Max	Units
On/Off Signal Interface (V_{IN}=V_{IN}, min to V_{IN}, max ; open collector or equivalent, Signal referenced to GND)						
Logic High (Module ON)						
Input High Voltage	All	VIH	0.61	0.65	0.69	V
Logic Low (Module OFF)						
Input Low Voltage	All	VIL	0.51	0.55	0.65	V
Turn-On Delay and Rise Times (V_{IN}=$V_{IN, nom}$, I_O=$I_{O, max}$, V_O to within ±1% of steady state)						
Case 1: On/Off input is enabled and then input power is applied (delay from instant at which VIN = VIN, min until Vo =10% of Vo, set)	All	T_{DELAY}		1.1		msec
Case 2: Input power is applied for at least one second and then the On/Off input is enabled (delay from instant at which Von/Off is enabled until Vo = 10% of Vo, set)	All	T_{DELAY}		1		msec
Output voltage Rise time (time for Vo to rise from 10% of Vo,set to 90% of Vo, set)	All	T_{RISE}		15		msec
Output voltage overshoot (startup) (TA = 25°C VIN= VIN, MIN to VIN, max, IO = IO, min to IO, max)					4	% $V_{O, set}$
Over Temperature Protection (See Thermal Considerations section)	All	T_{OT}		125		°C
PMBus Over Temperature Warning Threshold (*	All	T_{WARN}		110		°C
Input Undervoltage Lockout						
Turn-on Threshold	All			6		V_{DC}
Turn-off Threshold	All			5.5		V_{DC}
Hysteresis	All			0.5		V_{DC}
PGOOD (Power Good)						
Recommended pull-up circuit: 10 kΩ resistor with 3.3V supply	All			10		kΩ
Output Low voltage (20 mA Drive)	All				0.1	V
Output High voltage	All				0.7	V
Output Leakage (Vpad = 3.6 V)	All		-5		5	µA
Sink current capability into PGOOD pin	All			5	6	mA

* Over temperature Warning – Warning may not activate before alarm and unit may shutdown before warning.

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General Specifications

Parameter	Condition	Min	Typ	Max	Unit
Calculated MTBF (I_O=0.8$I_{o,\ max}$, T_A=40°C) Telecordia	All		166,087,525		Hours
Weight			2.6 g		g (oz.)

Digital Interface Specifications

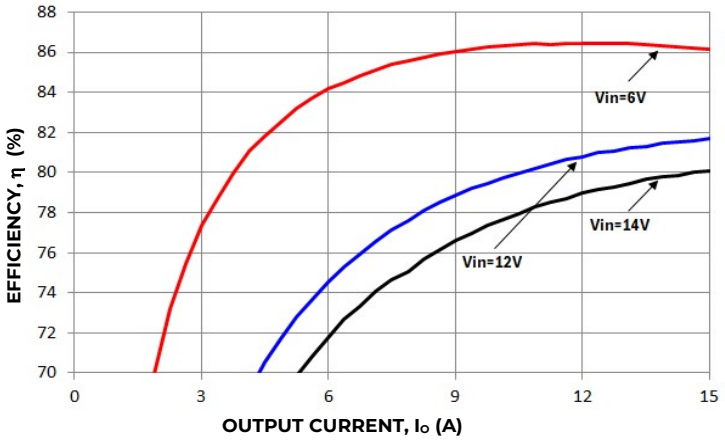
Unless otherwise indicated, specifications apply for all operating input voltages, resistive load and temperature conditions. See Feature Descriptions for additional information.

Parameter	Condition	Symbol	Min	Typ	Max	Unit
PMBus Signal Interface Characteristics						
Input High Voltage (SM_DATA, SM_ALERT)		V_{IH}	1.35			V
Input Low Voltage (SM_DATA, SM_ALERT)		V_{IL}			0.8	V
Input Leakage (SM_DATA, SM_CLK)	Vpad = 0 – 3.6V	I_{IH}	-1		1	µA
Output Low Voltage (Open-Drain Outputs – 4mA drive, SM_DATA, SM_ALERT)	I_{OUT}=4mA	V_{OL}			0.4	V
Pin capacitance		C_O		4		pF
PMBus Operating frequency range	Slave Mode	F_{PMB}	100	400	1000	kHz
Pulldown resistance (SM_DATA, SM_CLK)			5		13	Ω
Pulldown resistance (SM_ALERT)			5		20	Ω
Measurement System Characteristics						
Output current measurement range		$I_{OUT(rng)}$	0		15	A
Output current measurement accuracy	All	I_{ACC}		3.6		A
Temperature measurement accuracy @12V_{IN}, 0°C to 85°C		T_{ACC}	-1		1	°C
V_{IN} measurement range		$V_{IN(rng)}$	6		14.5	V
V_{IN} measurement accuracy		$V_{IN,\ ACC}$		±0.6		%
V_{IN} measurement resolution		$V_{IN,\ RES}$		31.25		mV
V_{OUT} measurement range		$V_{OUT(rng)}$	0.45		3.6	V
V_{OUT} measurement resolution		$V_{OUT(res)}$		0.244		mV
V_{OUT} measurement accuracy	V_{OUT}= 0.45 - 3.6	$V_{OUT,\ ACC}$		±2.5		%

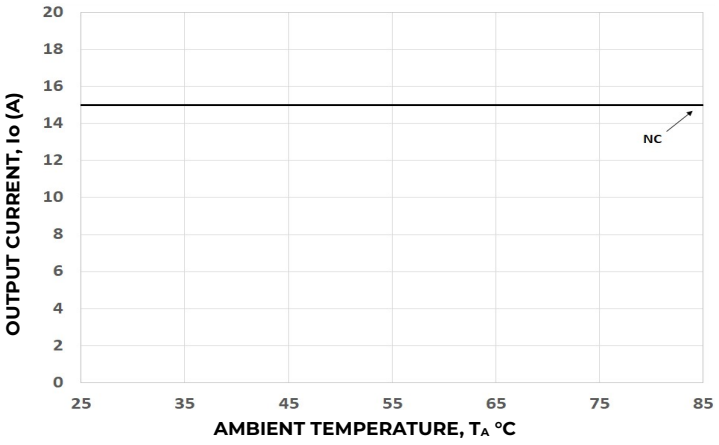
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Characteristic Curves

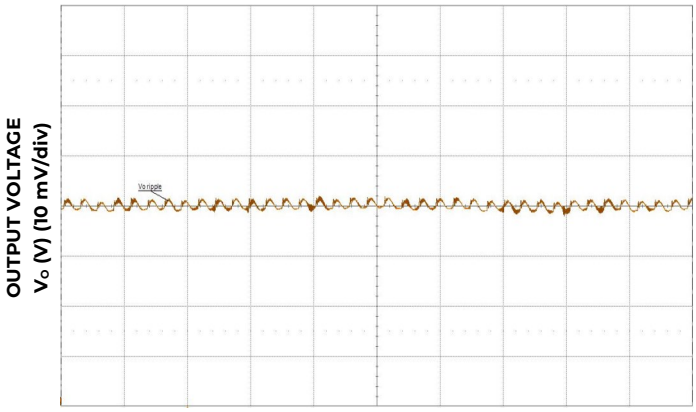
The following figures provide typical characteristics for the 15A DLynx III™ module at 0.45Vo and 25°C.



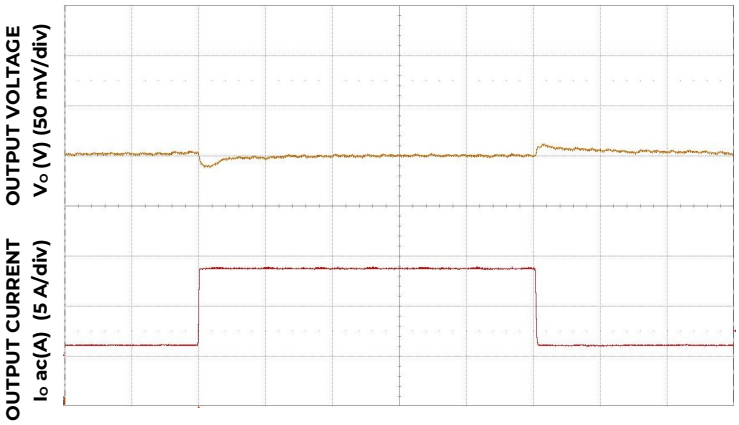
Converter Efficiency versus Output Current.



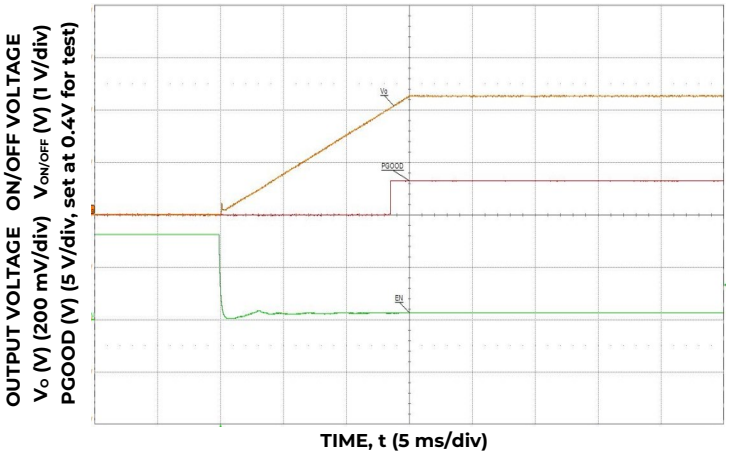
Derating Output Current versus Ambient Temperature and Airflow.



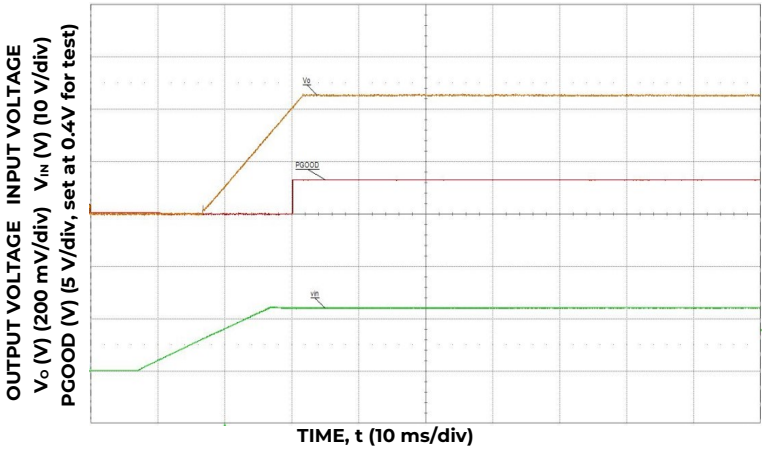
Typical output ripple
C_O=8x470uF+48x47uF+2x22uF+6x0.1uF, V_{IN} = 12V, I_o = $I_{o,max}$



Transient response to 10 A/µs Load Change from 25% to 75% at 12V_{IN}, Co=8x470uF+48x47uF+2x22uF+6x0.1uF



Typical Start-up Using On/Off Voltage
(I_o = $I_{o,max}$).

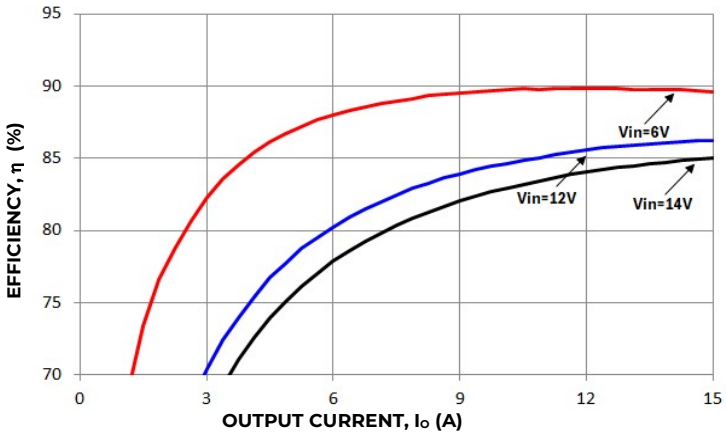


Typical Start-up Using Input Voltage
(V_{IN} = 12V, I_o = $I_{o,max}$).

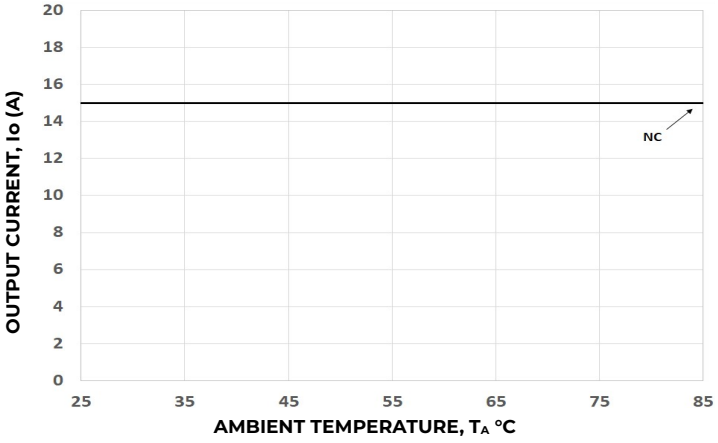
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Characteristic Curves

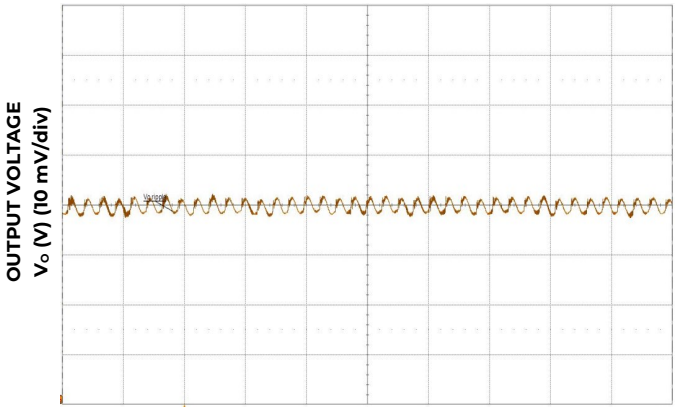
The following figures provide typical characteristics for the 15A DLynx III™ module at 0.7Vo and 25°C.



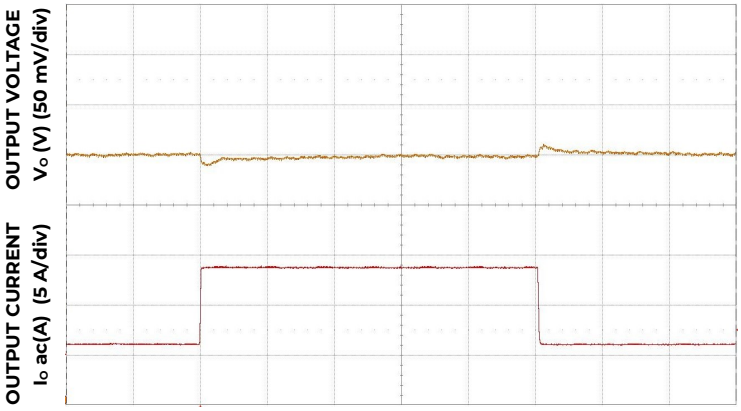
Converter Efficiency versus Output Current.



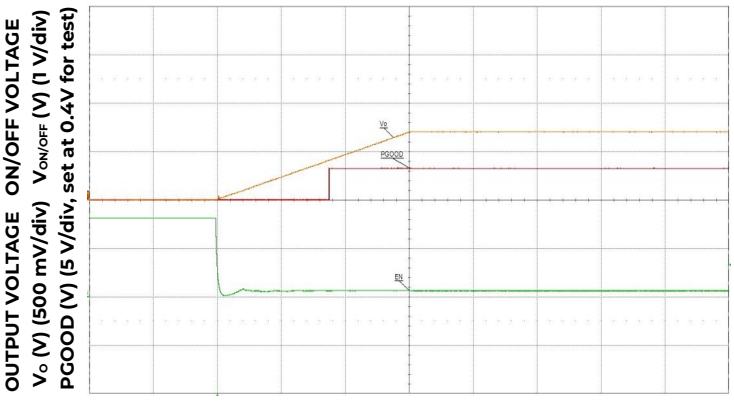
Derating Output Current versus Ambient Temperature and Airflow.



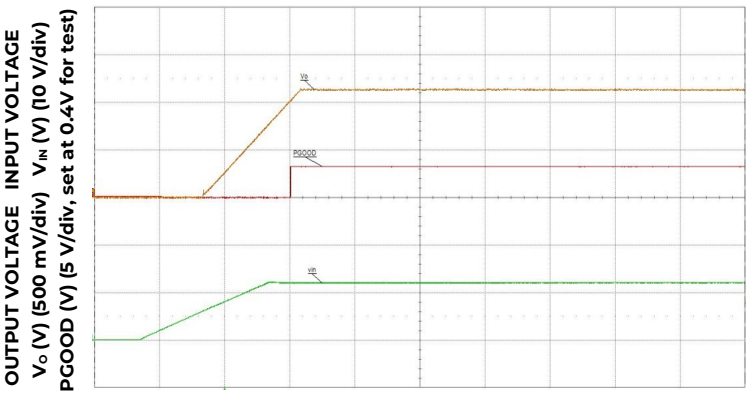
Typical output ripple
C_O=8x470uF+48x47uF+2x22uF+6x0.1uF, V_{IN} = 12V, I_o = $I_{o,max}$



Transient response to 10 A/µs Load Change from 25% to 75% at 12V_{IN}, Co=8x470uF+48x47uF+2x22uF+6x0.1uF



Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

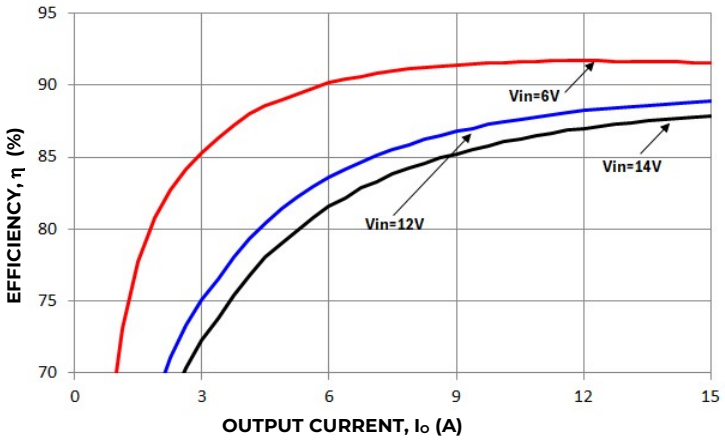


Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

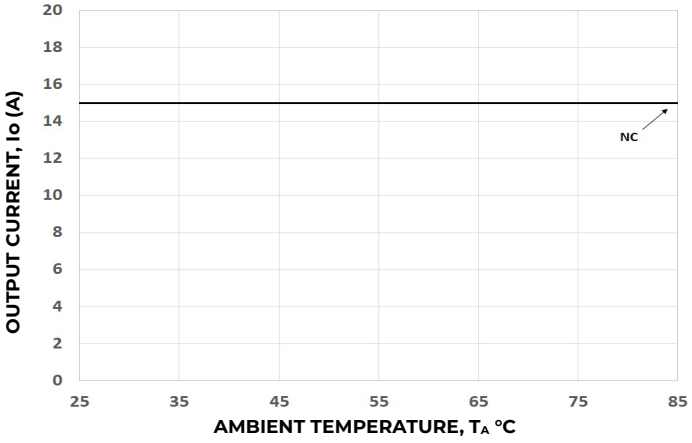
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Characteristic Curves

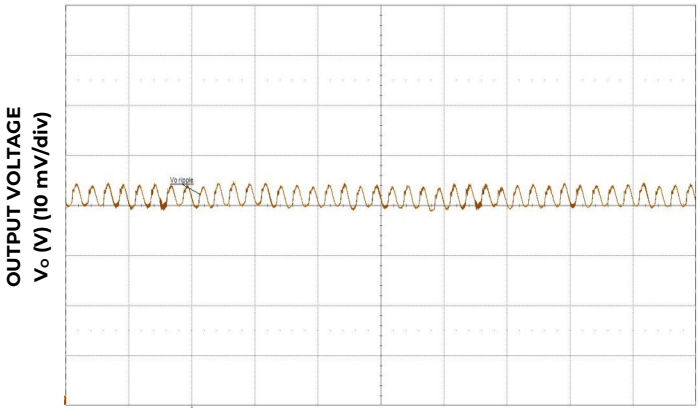
The following figures provide typical characteristics for the 15A DLynx III™ module at 1.0Vo and 25°C.



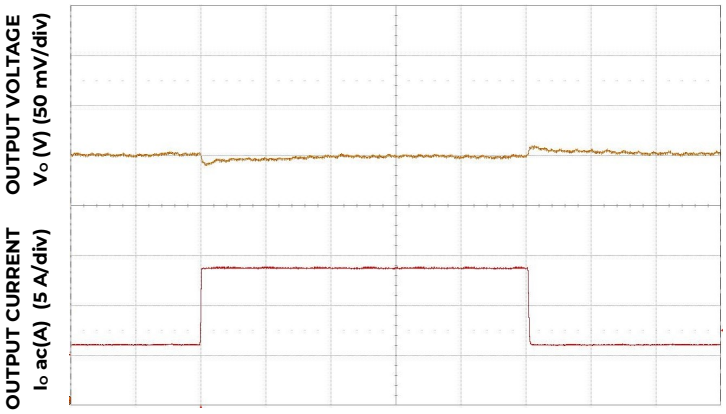
Converter Efficiency versus Output Current.



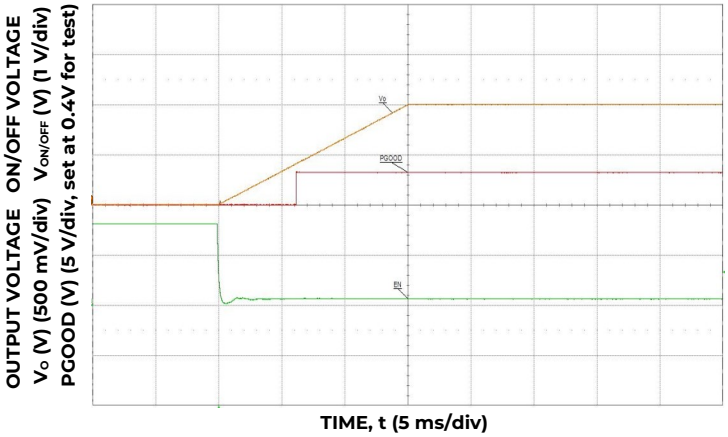
Derating Output Current versus Ambient Temperature and Airflow.



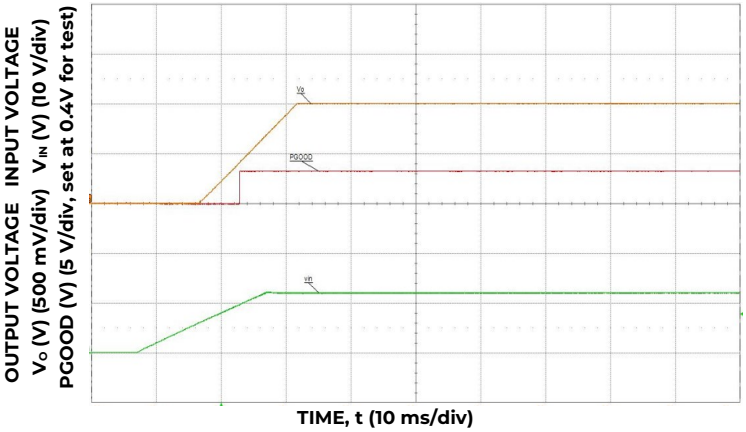
Typical output ripple
C_O=8x470uF+48x47uF+2x22uF+6x0.1uF, V_{IN} = 12V, I_o = $I_{o,max}$



Transient response to 10 A/µs Load Change from 25% to 75% at 12V_{IN}, Co=8x470uF+48x47uF+2x22uF+6x0.1uF



Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

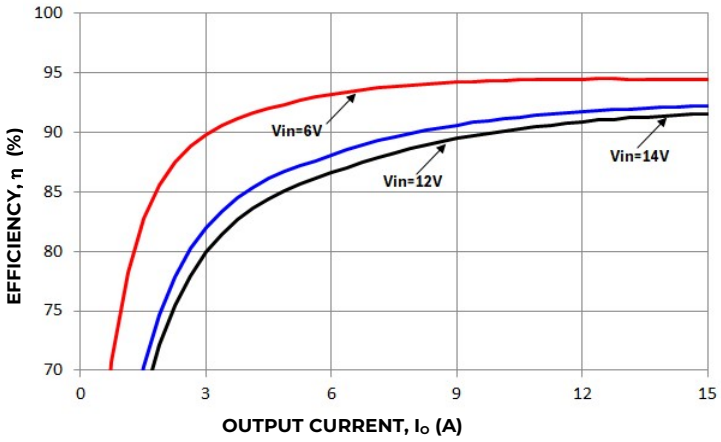


Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

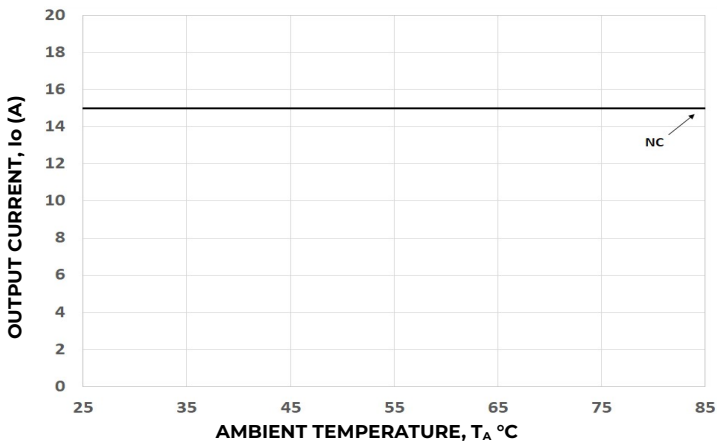
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Characteristic Curves

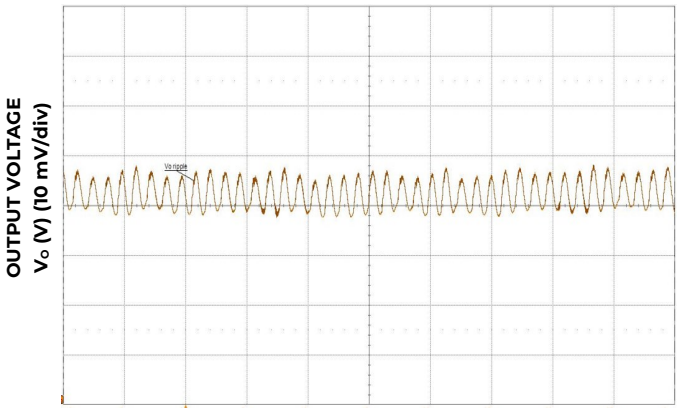
The following figures provide typical characteristics for the 15A DLynx III™ module at 2.0Vo and 25°C unless otherwise indicated.



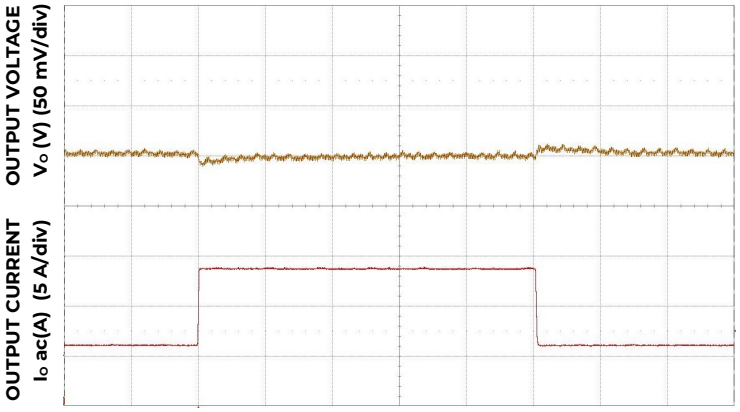
Converter Efficiency versus Output Current.



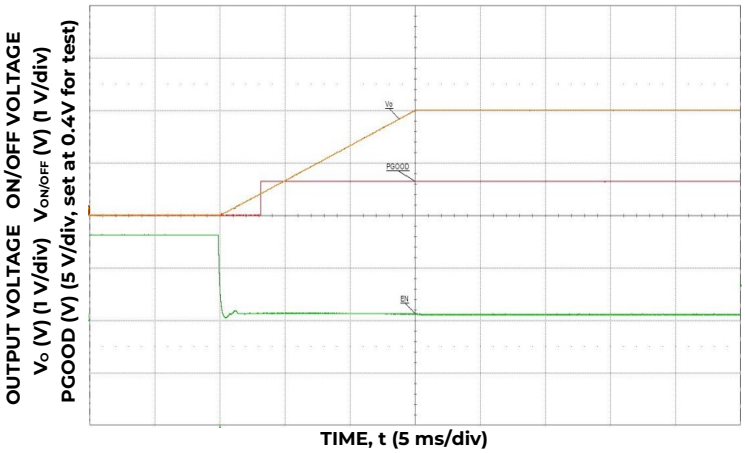
Derating Output Current versus Ambient Temperature and Airflow.



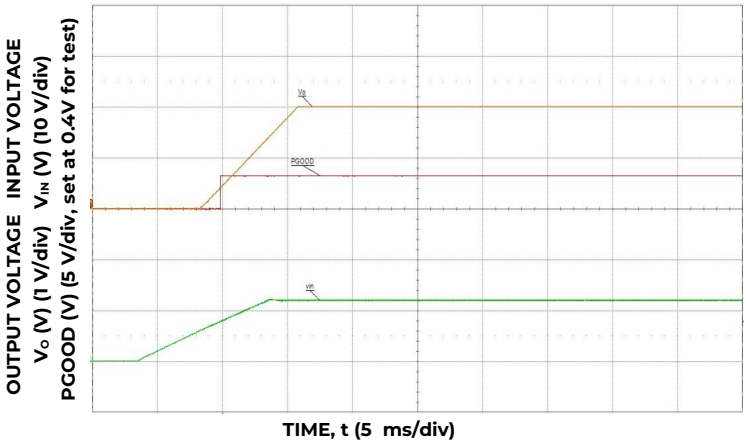
Typical output ripple
C_O=8x470uF+48x47uF+2x22uF+6x0.1uF, V_{IN} = 12V, I_o = $I_{o,max}$



Transient response to 10 A/µs Load Change from 25% to 75% at 12V_{IN}, Co=8x470uF+48x47uF+2x22uF+6x0.1uF



Typical Start-up Using On/Off Voltage
(I_o = $I_{o,max}$).



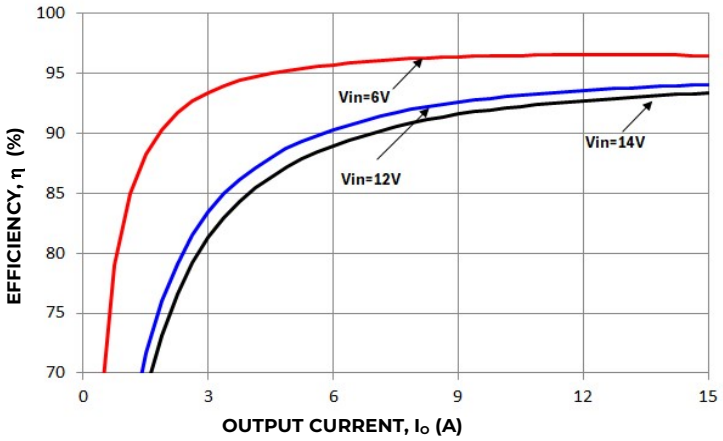
Typical Start-up Using Input Voltage
(V_{IN} = 12V, V_{OUT} = 1.8V, I_o = $I_{o,max}$).

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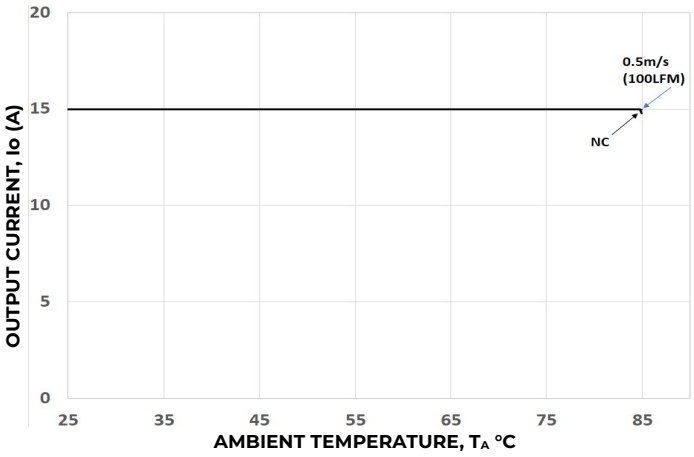
Technical Specifications (continued)

Characteristic Curves

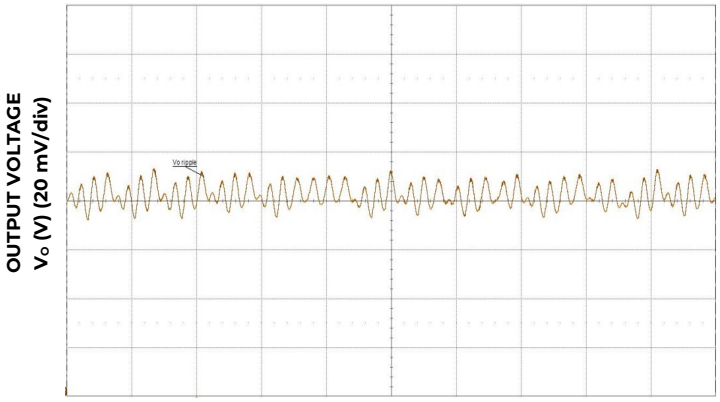
The following figures provide typical characteristics for the 15A DLynx III™ module at 3.6Vo and 25°C unless otherwise indicated.



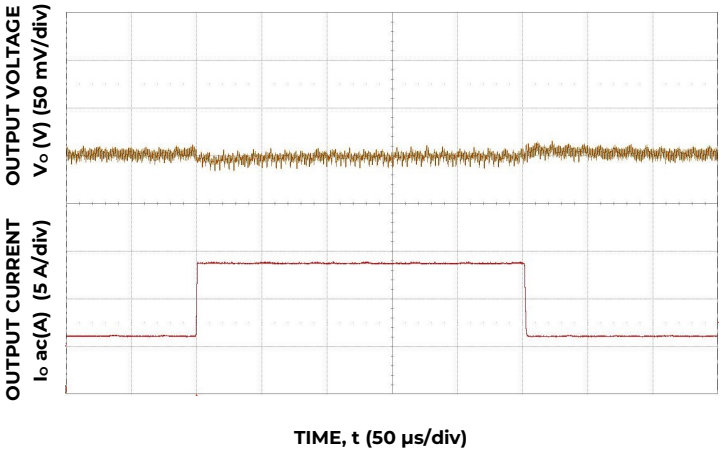
Converter Efficiency versus Output Current.



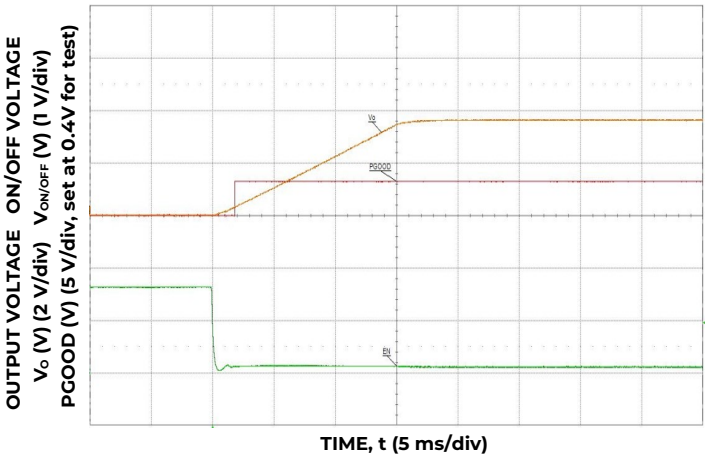
Derating Output Current versus Ambient Temperature and Airflow.



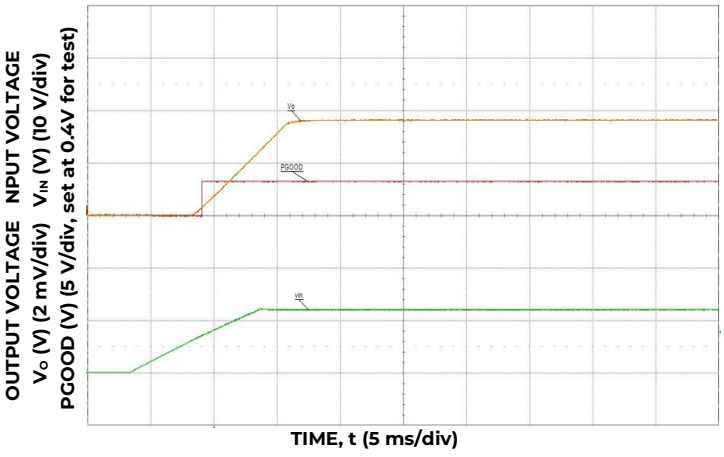
Typical output ripple
C_O=8x470uF+48x47uF+2x22uF+6x0.1uF, V_{IN} = 12V, I_o = $I_{o,max}$



Transient response to 10 A/µs Load Change from 25% to 75% at 12V_{IN}, Co=8x470uF+48x47uF+2x22uF+6x0.1uF



Typical Start-up Using On/Off Voltage
(I_o = $I_{o,max}$).

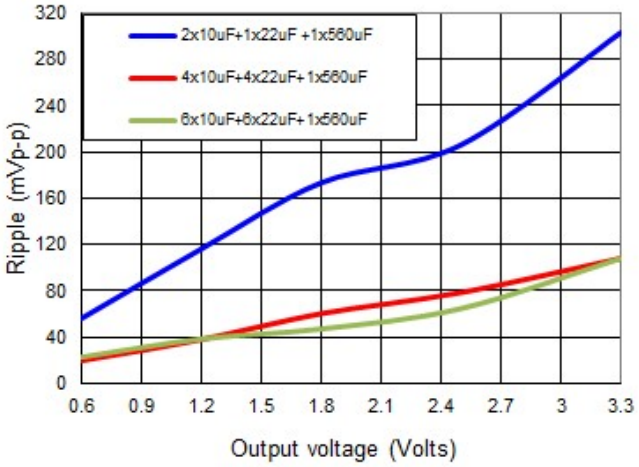


Typical Start-up Using Input Voltage
(V_{IN} = 12 V, V_{OUT} = 3.54 V I_o = $I_{o,max}$).

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Input Filtering

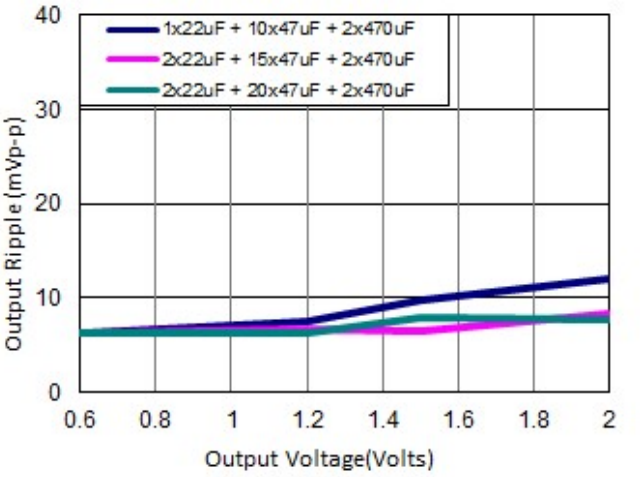
To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Figure below shows the input ripple voltage for various output voltages at 100% of load current with different input capacitor combinations.



Input ripple voltage for various output voltages with three input capacitor combinations at full load. Input voltage is 12V.

Output Filtering

These modules are designed for low output ripple voltage and will meet stringent output ripple. Next figure provides output ripple information various output voltages and full load current for different levels of capacitance. Ceramic capacitance deployed to reduce output ripple also helps improve the transient performance of the module.



Peak to peak output ripple voltage for various output voltages with external capacitors at the output (15 A load). Input voltage is 12V.

Transient Testing

Module performance for different transient conditions at CO=2x470uF+20x47uF+2x22uF+6x0.1uF measured on module evaluation board in room temperature (25° C) with 12 V_{DC} input voltage. VOUT_SCALE_LOOP value 0xE808 and no voltage divider used for 0.45 - 2.0 V output voltages. VOUT_SCALE_LOOP value 0xE804 used for higher VOUT.

Output Voltage (V)	Step Load of full load	Load Slew Rate (A/µsec)	ΔV Variation undershoot / overshoot (mV)
0.45	25% to 75%	10	-17 / 10
0.7	25% to 75%	10	-16 / 15
1.0	25% to 75%	10	-14 / 14
2.0	25% to 75%	10	-9 / 10
3.3	25% to 75%	10	-16 / 5
3.6	25% to 75%	10	-19 / 12
0.45	25% to 75%	2	-18 / 14
0.7	25% to 75%	2	-15 / 12
1.0	25% to 75%	2	-10 / 11
2.0	25% to 75%	2	-9 / 8
3.3	25% to 75%	2	-15 / 6
3.6	25% to 75%	2	-12 / 12

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Safety Considerations

For safety agency approval, the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL* 62368-1, 3rd Ed. Recognized, and VDE (EN62368-1, 3nd Ed.) Licensed.

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV) or ES1, the input must meet SELV/ES1 requirements. The power module has extra low voltage (ELV) outputs when all inputs are ELV.

The FPLX015 model was tested using an external Littelfuse 456 series fast-acting fuse rated at 30 A, 100 V in the ungrounded input. The maximum hot spot temperature on C5 shall shall not exceed 115 °C and on inductor core top shall not exceed 125°C.

Analog Feature descriptions

Remote On/Off

The FPLX015 module can be turned ON and OFF either by using the EN pin (Analog enable) or through the PMBus interface (Digital enable). The module can be configured in a number of ways through the PMBus interface to react to the ON/OFF input:

- Power up when power present ignoring EN pin and OPERATION (0x01) PMBus command.
- Power up by EN pin and OPERATION PMbus command (default)
- Power up with OPERATION PMbus command only.
- Power up with EN pin only

The default state of the module (as shipped from the factory) is to be controlled by both EN pin and OPERATION PMBus command . Module control through the digital interface must be made through PMBus. These changes can be made and written to non-volatile memory on the module so that it is remembered for subsequent use.

The EN pin should not be left floating and must be pulled either high or low.

Monotonic Start-up and Shutdown

The module has monotonic start-up and shutdown behavior on the output for any combination of rated input voltage, output current, and operating temperature range.

Startup into Pre-biased Output

The module will start into a pre biased output on output as long as the pre bias voltage is 10% less than the set output voltage at 25°C. 50% less than the set output voltage for all temperature conditions.

Remote Sense

The power module has a differential Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the sense pins (VOSENP and VOSENM) for the output. The maximum differential input voltage for the remote sense input is 2.56 V.

Setting output voltage with external resistor

15 pre-set VOUT values are selectable connecting a pinstrap resistor to boot voltage (VBT) pin. With pre-set VOUT selected with resistor on application board modules can be powered up without any PMBus commands.

For ≤2.0V Vout it is recommended to not use feedback resistor divider.

VBT and EN pins must not be left floating.

PROG RESISTOR	VOUT 0.45 – 2.0 Without feedback	VOUT 0.5 – 3.6 With feedback resistor
5.62 kΩ	0.5 V_{DC}	1.0 V_{DC}
9.53 kΩ	0.6 V_{DC}	1.2 V_{DC}
14 kΩ	0.7 V_{DC}	1.4 V_{DC}
21 kΩ	0.8 V_{DC}	1.6 V_{DC}
30.1 kΩ	0.9 V_{DC}	1.8 V_{DC}
36.5 kΩ	1.0 V_{DC}	2.0 V_{DC}
43.2 kΩ	1.05 V_{DC}	2.1 V_{DC}
51.1 kΩ	1.1 V_{DC}	2.2 V_{DC}
61.9 kΩ	1.2 V_{DC}	2.4 V_{DC}
75 kΩ	1.25 V_{DC}	2.5 V_{DC}
88.7 kΩ	1.35 V_{DC}	2.7 V_{DC}
105 kΩ	1.5 V_{DC}	3.0 V_{DC}
127 kΩ	1.65 V_{DC}	3.3 V_{DC}
147 kΩ	1.8 V_{DC}	3.6 V_{DC}

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Power Good

Power good needs external pull up resistor. The pin is called PGOOD and threshold is specified via PMbus (POWER_GOOD_ON and POWER_GOOD_OFF).

When using VBT pin for analog VOUT setting, FPLX015 will automatically set PGOOD ON threshold at 93.75% of VOUT set with VBT pin and PGOOD OFF threshold at 81.25% of VOUT.

When using PMBus command to set VOUT user can set PGOOD threshold with PMBus commands. If PGOOD is not set by user factory default setting is 0.4V.

Refer to the startup waveforms in characteristic curves section for examples of Power Good / PGOOD behavior. The top waveform is the slowly rising input voltage and the bottom waveform is the output voltage. As soon as the output voltage crosses the PGOOD threshold (0.4V by default), the pin is pulled high as seen in the scope capture (red middle waveform).

Start-up procedure

The FPLX015A0XY3-SRZ is a programmable ON/OFF logic power module. The default state of the module is Negative Logic. The module is ON when the EN pin is at “logic low” state, and OFF when it is at a “logic high” state. Positive ON/OFF logic can be implemented through PMBus control.

The module could be turned ON and OFF from an external enable signal or by the OPERATION (0x01) command. Desired behavior is set by ON_OFF_CONFIG (0x02) command.

Input overvoltage protection (OVP)

The input overvoltage protection prevents the FPLX015A0XY3-SRZ from operating when the input is above preset thresholds.

The customers are strongly advised not to increase the preset input overvoltage limit as it may result in compromising product safety. This is a violation of the module’s absolute maximum and minimum ratings which will void the product warranty.

The input overvoltage protection could be adjusted by the following command:

VIN_OV_FAULT_RESPONSE 0x56.

VIN_OV_FAULT_LIMIT 0x55

See PMBus commands description for more details.

Output overvoltage and undervoltage protections

The FPLX015A0XY3-SRZ offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits.

The FPLX015A0XY3-SRZ overvoltage and undervoltage behavior can be configured through the following commands:

VOUT_OV_FAULT_RESPONSE (0x41),
VOUT_UV_FAULT_RESPONSE (0x45),
VOUT_OV_FAULT_LIMIT (0x40),
VOUT_UV_FAULT_LIMIT (0x44).

See commands description for more details.

Output overcurrent protection (OCP)

To provide protection in a fault (output overload) condition, the unit is equipped with internal current limiting circuitry on the output and can endure current limiting continuously.

FPLX015 module has two output overcurrent protections to prevent excessive forward current through the module and the load during abnormal operation. Internal overcurrent protection is cycle-by-cycle in nature. Second over current protection mode is based on average current and managed by IOUT_OC_FAULT_LIMIT 0x46.

Preset output overcurrent limit must not be increased as it may result in compromising product safety. This is a violation of the module’s absolute maximum and minimum ratings which will void the product warranty.

The output overcurrent fault response is managed by the PMBus command IOUT_OC_FAULT_RESPONSE (0X47). The module’s default overcurrent response is to hiccup forever. Other PMBus selectable OCP responses are shutdown or hiccup 1 to 6 times before shutdown. Time delay to next retry can be set between 1 - 8 msec. See PMBus commands description for more details.

Thermal shutdown circuit

To provide protection in a fault condition, the unit has a thermal shutdown circuit. The unit will shut down if the overtemperature threshold of 125 °C is exceeded. IC internal temperature can be read with PMBus command READ_TEMPERATURE_1. Once the unit goes into thermal shutdown, it will wait to cool down to 110°C of set limit before attempting to restart.

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Overtemperature protection (OTP)

The FPLX015A0XY3-SRZ overtemperature protection ensures that the temperature inside the module is below all the components' temperature maximum limit.

The overtemperature protections are managed by the following PMBus commands: OT_FAULT_LIMIT, OT_WARN_LIMIT, and OT_FAULT_RESPONSE.

The module supports two responses: ignore and restart when fault condition clears. The fault is non-latching, when temperature lowers to OT_WARN_LIMIT module will restart.

Preset over temperature limit must not be decreased as it may result in compromising product safety. This is a violation of the module's absolute maximum and minimum ratings which will void the product warranty.

See PMBus commands description for more details.

Monitoring through SM_ALERT pin

The FPLX015A0XY3-SRZ controller can report fault conditions by changing the state of the SM_ALERT pin, which is asserted when any number of preconfigured fault conditions occur. The module can also be monitored continuously for any number of power conversion parameters. Some of most useful fault monitoring commands are: STATUS_BYTE 0x78, STATUS_WORD 0x79, STATUS_VOUT 0x7A, STATUS_IOUT 0x7B, STATUS_INPUT 0x7C, STATUS_TEMPERATURE 0x7D

Control loop tuning

The heart of FPLX015A0XY3-SRZ is a fully digital fast Constant On Time controller IC . By default, this control loop is stable for minimum recommended output capacitance and loads. One at least 10 mΩ ESR COUT capacitor is required. There is no dependence upon external compensation networks. This simplifies the design process by removing such considerations as temperature and process variation of passive components.

Non-volatile memory management (NVM)

The FPLX015A0XY3-SRZ has internal non-volatile memory where the module's configurations are stored.

During the initialization process, the FPLX015A0XY3-SRZ checks for stored values contained in its internal non-volatile memory. The FPLX015 offers up to 11 writes to configure basic module parameters such as output voltage setpoint, fault operation settings, etc. Digital Power Insights ProGUI III software can show number of NVM writes available.

Reducing jitter in high V_{OUT} conditions

Some amount of jitter is unavoidable in any DCDC power conversion. Jitter is caused by noise that is present at the modulator which controls the operation of the power switches used to convert power. It results in mild Vout ripple increase. Fast COT control has fixed Ton time, consequently, its jitter is in the form of Toff time variation from cycle by cycle.

There are two approaches to reduce jitter:

- Increase equivalent series resistance (ESR) in Cout to make phase margin bigger, also the higher the ESR, the larger the feedback ripple, resulting in better noise rejection. (At least 10mΩ ESR is recommended).
- Adjust internal loop capacitance value (range from 1pF to 8pF) by changing PMBus command LOOP_COMPENSATION_FILTER_ZERO_0 to aid with the crossover frequency and provide a phase boost.

Fast Constant On Time control scheme

The FPLX015 module uses constant on time control scheme to regulate the output voltage. As with all POL modules, external capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise and to reduce output voltage deviations from the steady-state value in the presence of dynamic load current changes.

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PMBus use guidelines

An I²C or PMBus interface is used to communicate with the module. These two-wire serial interfaces consist of clock and data signals, and operate as fast as 1 MHz with proper signal integrity. 400kHz is the typical operating frequency. The bus provides read and write access to the internal registers for configuration and monitoring of operating parameters. The bus is also used to program on-chip non-volatile memory (MTP) to store operating parameters. To ensure operation with multiple devices on the bus, an exclusive address for the module is programmed into MTP. To protect customer configuration and information, the I²C interface can be configured for either limited access or locked with a 16 -bit software password. Limited access includes both write and read protection options. In addition, there is a telemetry-only mode which only allows reads from the telemetry registers. The module supports the Packet Error Checking (PEC) protocol and a number of PMBus commands to monitor voltages and currents.

PMBus data formats

Linear-11

The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent a real world decimal value (X). The formula to calculate the real world decimal value is: $X = Y \cdot 2^{N}$.

Linear-16

The L16u data format uses a fixed exponent (hard-coded to N = -xxh) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). The formula to calculate the real world decimal value is: $X = Y \cdot 2^{-xx}$.

Linear-16 Signed

The L16s data format uses a fixed exponent (hard-coded to N = -xxh) and a 16-bit two's complement mantissa (Y) to represent real world decimal value (X). The formula to calculate the real world decimal value is: $X = Y \cdot 2^{-xx}$.

Bit Field

A description of the Bit Field format is provided in each command details.

Custom

A description of the Custom data format is provided in each command details. A combination of Bit Field and integer are common type of Custom data format.

ASCII (ASC)

A variable length string of text characters in the ASCII data format.

PMBus Addressing

The power module is addressed through the PMBus using a device address. The default module address is 0x40.

PMBus default address can be changed with PMBus command PMB_DEVICE_ADDR to a new value. Setting the address to zero disables the interface.

PMBUs default address can also be changed with pinstrap resistor to an offset address. The module supports 15 possible offset addresses (0x41 to 0x56). Connect pinstrap resistor to PRG pin.

PROG PIN RESISTOR	PMBus address offset from default 0x40
SHORT	0 (0x40- default)
5.62 kΩ	1
9.53 kΩ	2
14 kΩ	3
21 kΩ	4
30.1 kΩ	5
36.5 kΩ	6
43.2 kΩ	7
51.1 kΩ	8
61.9 kΩ	9
75 kΩ	10
88.7 kΩ	11
105 kΩ	12
127 kΩ	13
150	14
FLOAT	15 (0x56)

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Supported PMBus Commands

This section provides a list of supported PMBus commands outlined in the order of increasing command codes. More information about standardized PMBus electrical interface, commands, data formats and command language can be found from http://pmbus.org/ and at http://www.smbus.org/specs/. This data sheet does not re-address all of the details contained within the key PMBus Specification documents listed below.

Specification Part I – General Requirements Transport And Electrical Interface

Includes the general requirements, defines the transport and electrical interface and timing requirements of hardwired signals.

Specification Part II – Command Language

Describes the operation of commands, data formats, fault management and defines the command language used with the PMBus.

System Management Bus Specification, Version 2.0, August 3, 2000

This specification specifies the version of the SMBus on which Revision 1.3 of the PMBus Specification is based. PMBus Specification Part I and II can be requested from PMBus website. System management bus specification can be

Supported PMBus Commands

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	UNIT	TRANSFER TYPE	DEFAULT VALUE	MIN/MAX VALUES or RANGE
PAGE	0x00	1	bit field		R/W	0x00	0x00
OPERATION	0x01	1	bit field		R/W	0x80	0x00/40/80/94/98/A4/A8
ON_OFF_CONFIG	0x02	1	bit field		R/W	0x1D	0x02/14/15/16/17/18/1C/1D/1E/1F
CLEAR_FAULTS	0x03	1			W		
WRITE_PROTECT	0x10	1	bit field		R/W	0x00	0x80/40/20/03/02/00
STORE_USER_ALL	0x15	1			W		
RESTORE_USER_ALL	0x16	1			W		
CAPABILITY	0x19	1	bit field		R	0xD0	
SMBALERT_MASK	0x1B	5	bit field		R/W	0x0000000000	
VOUT_MODE	0x20	1	mode+exp		R/W	0x14 (-12)	0x14/15/16/17/18
VOUT_COMMAND	0x21	2	16-bit linear	V	R/W	0x1000 (1.0 V)	0.4 to 2.0/(0.5 to3.6 with FB divider)
VOUT_MAX	0x24	2	16-bit linear	V	R/W	0x2400 (2.25 V)	0.4 to 2.25/(0.5 to3.7 with FB divider)
VOUT_MARGIN_HIGH	0x25	2	16-bit linear	V	R/W	0x4301 (1.05 V)	0.45 to 2.2/(0.5 to 3.6 with FB divider)
VOUT_MARGIN_LOW	0x26	2	16-bit linear	V	R/W	0x3891 (0.95 V)	0.45 to 2.2/(0.5 to 3.6 with FB divider)
VOUT_TRANSITION_RATE	0x27	2	11-bit linear	mV/us	R/W	0xE808 (1 mV/us)	0 to 127.875
VOUT_DROOP	0x28	2	11-bit linear	mΩ	R/W	0x0000 (0 mΩ)	0 to 9.98/(0 to 49.9)
VOUT_SCALE_LOOP	0x29	2	11-bit linear		R/W	0x808 (1:1 ratio)	0xE808/0xE804
VOUT_MIN	0x2B	2	16-bit linear	V	R/W	0x0400 (0.25 V)	0 to 3.7
FREQUENCY_SWITCH	0x33	2	11-bit linear	kHz	R/W	0x0320 (800 Khz)	600/800/1000
VIN_ON	0x35	2	11-bit linear	V	R/W	0xF80C (6.0 V)	6 to 14
VIN_OFF	0x36	2	11-bit linear	V	R/W	0xF80B (5.5 V)	5.5 to 14
VOUT_OV_FAULT_LIMIT	0x40	2	16-bit linear	V	R/W	0x2333 (2.2 V)	0.4 to 2.2
VOUT_OV_FAULT_RESPONSE	0x41	1	bit field		R/W	0xBF (Shutdown/retry)	0x00/(0x80 - 0xBF)
VOUT_UV_FAULT_LIMIT	0x44	2	16-bit linear	V	R/W	0x0666 (0.4 V)	0.4 to 2.2
VOUT_UV_FAULT_RESPONSE	0x45	1	bit field		R/W	0xBF (Shutdown/retry)	0x00/(0x80 -0xBF)

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Digital Feature Descriptions (continued)

Supported PMBus Commands (continued)

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	UNIT	TRANSFER TYPE	DEFAULT VALUE	MIN/MAX VALUES or RANGE
VOUT_UV_FAULT_LIMIT	0x44	2	16-bit linear	V	R/W	0x0666 (0.4 V)	0.4 to 2.2
VOUT_UV_FAULT_RESPONSE	0x45	1	bit field		R/W	0xBF (Shutdown/retry)	0x00/(0x80 -0xBF)
IOUT_OC_FAULT_LIMIT	0x46	2	11-bit linear	A	R/W	0xE120 (18 A)	0 to 18
IOUT_OC_FAULT_RESPONSE	0x47	1	bit field		R/W	0xFF (Shutdown/retry)	0xC0 to 0xFF
OT_FAULT_LIMIT	0x4F	2	11-bit linear	°C	R/W	0x007D (125°C)	0 to 125
OT_FAULT_RESPONSE	0x50	1	bit field		R/W	0xF8 (Restart)	0x00/(0xC0 -0xBF)
OT_WARN_LIMIT	0x51	2	11-bit linear	°C	R/W	0x006E (110°C)	0 to 124
VIN_OV_FAULT_LIMIT	0x55	2	11-bit linear	V	R/W	0xE0E8 (14.5 V)	6 to14.5
VIN_OV_FAULT_RESPONSE	0x56	1	bit field		R/W	0x80 (Shutdown)	0x00/(0x80 - 0xBF)
POWER_GOOD_ON	0x5E	2	16-bit linear	V	R/W	0x0666 (0.399 V)	0.3 to 2.0/(0.3 to3.6 with FB divider)
POWER_GOOD_OFF	0x5F	2	16-bit linear	V	R/W	0x0666 (0.399 V)	0.3 to 2.0/(0.3 to3.6 with FB divider)
TON_DELAY	0x60	2	11-bit linear	ms	R/W	0x0000 (0 ms)	0 - 127.5
TON_RISE	0x61	2	11-bit linear	ms	R/W	0xF81E (15 ms)	0 - 127.5
TOFF_DELAY	0x64	2	11-bit linear	ms	R/W	0x0000 (0 ms)	0 - 127.5
TOFF_FALL	0x65	2	11-bit linear	ms	R/W	0xF81E (15 ms)	0 - 127.5
STATUS_BYTE	0x78	1	bit field		R/W	0x00	
STATUS_WORD	0x79	2	bit field		R/W	0x0000	
STATUS_VOUT	0x7A	1	bit field		R/W	0x00	
STATUS_IOUT	0x7B	1	bit field		R/W	0x00	
STATUS_INPUT	0x7C	1	bit field		R/W	0x00	
STATUS_TEMPERATURE	0x7D	1	bit field		R/W	0x00	
STATUS_CML	0x7e	1	bit field		R/W	0x00	
READ_VIN	0x88	2	11-bit linear	V	R	Vary	
READ_IIN	0x89	2	11-bit linear	A	R	Vary	
READ_VOUT	0x8B	2	11-bit linear	V	R	Vary	
READ_IOUT	0x8C	2	11-bit linear	A	R	Vary	
READ_TEMPERATURE_1	0x8D	2	11-bit linear	°C	R	Vary	
READ_POUT	0x96	2	11-bit linear	W	R	Vary	
READ_PIN	0x97	2	11-bit linear	W	R	Vary	
PMBUS_REVISION	0x98	1	bit field		R	0x33	
MFR_ID	0x99	2	bit field		R	0x4F50 ("OP")	OmniOn Power (“OP”)
MFR_MODEL	0x9A	2	bit field		R	0x1E	
MFR_REVISION	0x9B	2	bit field		R	0x2025	
MFR_VENDOR_INFO_2	0xC2	2	bit field		R	Vary	
MFR_REG_ACCESS	0xD0	7	bit field		R/W	Vary	Allows users to access I2C register map based advanced commands. Supported I2C register map accessible commands are shown in Advanced Commands table.

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Advanced commands

This section provides a list of features accessible through MFR_REG_ACCESS (0xD0) PMBus command.
Read process is through following format:

S	PMBus address	W	A	Command 0xD0	A	Low register access	A	High Register Access	A	
Sr	PMBus address	R	A	Low Data Byte	A	High Data Byte	A*	PEC*	N	P

Write process is through following format:

S	PMBus	W	A	Command 0xD0	A	4	A	Low Register	A	High Register
- - - - - - - - - - -		A	Low Data Byte	A	High Data Byte		PEC	A	P	

S start condition, Sr repeated start condition, W write (0'), R read (1')
A acknowledge (0'), N not acknowledge (1'), P stop condition
* Present if PEC (Packet Error Correction) is enabled

Master to Slave	Slave to Master

Through the 0xD0 command user can access several advanced features. These features are:

Advanced Commands

Command name	Addr. offset	Address	Default Value	Valid Values	Description
fccm_mode	D0 005C	0x005C [1:1]	1	0--> DCM mode during light load 1--> CCM mode during light load	set this to force CCM mode
i2C_device_addr	D0 0040	0x0040 [14:8]	0x10	7-bit address, (0x00 - 0xFF) Reserved:0x00~0x07,0x08,0x0C,0x28,0x37,0x61,0x78~0x7F	sets the I2C device address, all registers at this address are protected by the i2c_pmb_addr_lock register
pmb_device_addr	D0 0040	0x0040 [6:0]	0x40	0x00 - 0xFF	the module pmbus address. Setting the address to zero disables the interface All registers at this address are protected by the i2c_pmb_addr_lock register
I2C/PMBUS Address lock	D0 00D4	0x00D4 [2:2]	1	0--> Disable Address Change 1--> Enable Address Change	
relative_ovp_thresh_en	D0 005E	0x005E [15:15]	1	0--> use Vout_OV threshold in PMBus 1--> User register Relative_ovp_threshold	Use register relative_ovp_thresh to specify the OVP threshold. This register overrides the PMBus commands. By default, PMBus commands control the VOUT OV and UV thresholds. Set this bit to use register relative_ovp_thresh to specify the OV/UV threshold instead.

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Digital Feature Descriptions (continued)

Advanced Commands (continued)

Command name	Addr. offset	Address	Default Value	Valid Values	Description
relative_ovp_thresh	D0 005E	0x005E [14:12]	3	Vout_scale_loop= 1:1 7-->400mV 6-->350mV 5-->300mV 4-->250mV 3-->200mV 2-->150mV 1-->100mV 0-->50mV vout_scale_loop= 1:2 7-->800mV 6-->700mV 5-->600mV 4-->500mV 3-->400mV 2-->300mV 1-->200mV 0-->100mV	specify the relative OVP threshold
fixed_ovp_thresh	D0 0060	0x0060 [2:0]	6	vout_scale_loop= 1:1 7-->Reserved 6-->2.2V 5-->1.8V 4-->1.5V 3-->1.35V 2-->1.2V 1-->1.0V 0-->0.8V vout_scale_loop= 1:2 7-->reserved 6-->4.4V 5-->3.6V 4-->3.0V 3-->2.7V 2-->2.4V 1-->2.0V 0-->1.6V	(cot) Fixed (pre-) ovp threshold control bits
relative_uvp _thresh_en	D0 005E	0x005E [11:11]	1	0--> use Vout_UV threshold in PMBus 1--> User register Relatvie_uvp_threshold	Use register relative_uvp_thresh to specify the UVP threshold. This register overrides the PMBus commands.
relative_uvp _thresh	D0 005E	0x005E [10:8]	3	Vout_scale_loop= 1:1 7-->400mV 6-->350mV 5-->300mV 4-->250mV 3-->200mV 2-->150mV 1-->100mV 0-->50mV vout_scale_loop= 1:2 7-->800mV 6-->700mV 5-->600mV 4-->500mV 3-->400mV 2-->300mV 1-->200mV 0-->100mV	Specify the relative UVP threshold.

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Digital Feature Descriptions (continued)

Advanced Commands (continued)

Command name	Addr. offset	Address	Default Value	Valid Values	Description
rovp_override_pin	D0 005E	0x005E [7:7]	0	0-->Set relative OVP and UVP thresholds from VBT pin 1-->Ignore the VBT pin, use PMBus command to set relative OVP and UVP	Setting this bit as 1 will ignore the VBT pin, use the PMbus command or registers relative_[ovp,uvp] _thresh to set OVO and UVP thresholds
fovp_override_pin	D0 005E	0x005E [6:6]	0	0-->Set fixed OVP and UVP thresholds from VBT pin 1-->Ignore the VBT pin, use PMBus command to set fixed OVP and UVP	Setting this bit as 1 will ignore the VBT pin, use register fixed_ovp_threshold
vboot_override_pin	D0 005E	0x005E [3:3]	0	0-->set initial target Vout voltage from VBT pin 1-->Ignore the VBT pin, use the VOUT_COMMAND (PMbus) to specify Initial target Vout voltage	Setting this bit as 1 will ignore the VBT pin, use the Vout_command value (PMbus mode) to specify the intial target Vout voltage
disable_relative_ovp	D0 0060	0x0060 [15:15]	0	0--> Enable relative ovp comparator 1--> disable relative ovp comparator, use fixed OVP threshold all the time	Setting this bit as 1 will ignore the relative OVP comparator. Use the fixed OVP threshold at all times
disable_relative_uvp	D0 0060	0x0060 [14:14]	0	0--> Enable relative uvp comparator 1--> disable relative uvp comparator, use fixed UVP threshold all the time	Setting this bit as 1 will ignore the relative UVP comparator
Loadline_range_sel	D0 006A	0x006A [6:6]	0	0 --> loadline range 0 ~ 10 mΩ 1--> loadline range 0 ~ 50 mΩ	The loadline resistance is 0-10 mΩ by default. Set this register to extend the resistance by 5X
loadline_current_sel	D0 006A	0x006A [5:4]	0	2,3--> output current(via ACD) 1 --> mean synthesized output current 0--> synthesized output current	Select the source of the output current for the loadline.
loadline_bandwidth	D0 006A	0x006A [3:0]	0	Register Value Range: 0 ~ 15; filter bandwidth=(1 + reg_value) * 30KHz	Loadline bandwidth, [u-4.9]. Controls the bandwidth of a filter that sits between the loadline voltage calculation and DAC. In general, this value should be set as low as it can go without hurting transient response. The filter bandwidth is (1 + reg_value) * 30KHz
cot_mintoff_ sel	D0 006E	0x006E [10:8]	1	7-5-->150 ns 4--> 200 ns 3--> 270 ns 2--> 340 ns 1--> 400 ns 0--> 470 ns	(cot) Programmable minimum off time.

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Digital Feature Descriptions (continued)

Advanced Commands (continued)

Command name	Addr. offset	Address	Default Value	Valid Values	Description
Loop_compensation_filter_zero_0	D0 0064	0x0064 [14:12]	6	Register Value Range: 0 ~ 7	loop compensation filter zero values
read_protect _mode	D0 0070	0x0070 [5:5]	0	0--> protection is enabled/ disabled by the USER password 1--> protection is always enabled (the USER password is ignored)	Select the read protection mode for the CNFG, TRIM and USER sections of the REGMAP. 0= protection is enabled/disabled by the USER password. 1= protection is always enabled (the USER password is ignored)
write_protect _mode	D0 0070	0x0070 [4:4]	0	0--> protection is enabled/ disabled by the USER password 1--> protection is always enabled (the USER password is ignored)	Select the write protection mode for the USER section of the REGMAP. write_protect_mode applies only to the USER section (the TRIM section is write-protected by the TRIM password).
read_protect _section	D0 0070	0x0070 [3:2]	0	3--> all Registers 2--> all except telemetry registers 1--> configuration (CNFG,TRIM,and User registers backed by OTP) 0--> None	Select the REGMAP section to be read-protected. Reads from protected registers return 0xFFFF. read_protect_section applies to all sections (CNFG, TRIM and USER). Note that only the USER password is used for read protection, and it applies to CNFG, TRIM and USER sections. The TRIM password is used for write protection only.
write_protect _section	D0 0070	0x0070 [1:0]	0	3--> all Registers 2--> all registers except VOUT_COMMAND 1--> configuration(CNFG and User registers backed by OTP) 0--> None	Select the REGMAP section to be write-protected. Writes to protected registers will be silently ignored. write_protect_section applies to the USER and CNFG sections. The TRIM section is write-protected by the TRIM password.
user_password	D0 007A	0x007A [15:0]	0xFFFF	0x0000 - 0xFFFF	A 16 bit password that provides read/ write protection for the USER section in all REGMAPs. Password protection is enabled by the Protect Section and Protect Mode registers. This register resets to zero, which is the default password. Once the password is set, access protection is enabled until user_try_password is set to the same value.
user_try_password	D0 00DA	0x00DA [15:0]	0x0000	0x0000 - 0xFFFF	used to unlock user registers

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Power Module Wizard

Designers can access a free, web-based, easy to use tool that helps users simulate FPLX015A0XY3-SRZ performance in selected application conditions (V_{IN}, V_{OUT}, I_{MAX}, transient event, etc.) . Go to **omnionpower.com** and sign up for a free account to use the module selector tool. The tool also offers online Simplis/Simetrix models that can be used to assess transient performance, efficiency, ripple, etc. Tool also generates a schematic and BOM with needed few external components (C_{OUT}) that can be downloaded along with the simulation results.

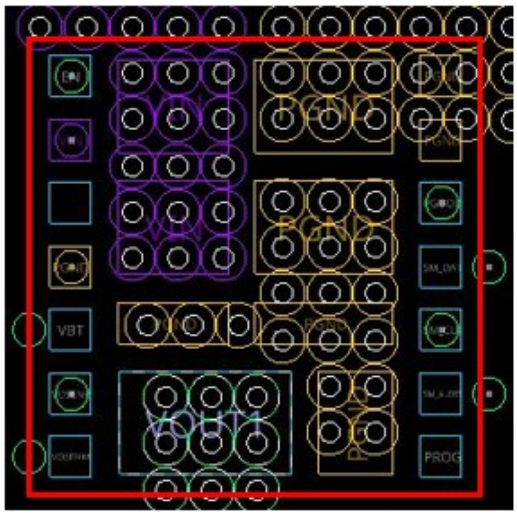
Digital Power Insights (DPI) ProGUI III

DPI is a software tool that helps users evaluate and simulate the PMBus performance of the FPLX015A0XY3-SRZ modules without the need to write software. The software can be downloaded for free from our webpage. A USB to I^2C adapter and associated cable set are required for proper functioning of the software suite. For first time users, we recommend using the DPI Evaluation Kit, which can be purchased from any of the leading distributors. Please ensure that the USB to I^2C adapter being used/ purchased is Version 2.2 or higher. Part Numbers are available in the last few pages of this datasheet

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Layout considerations

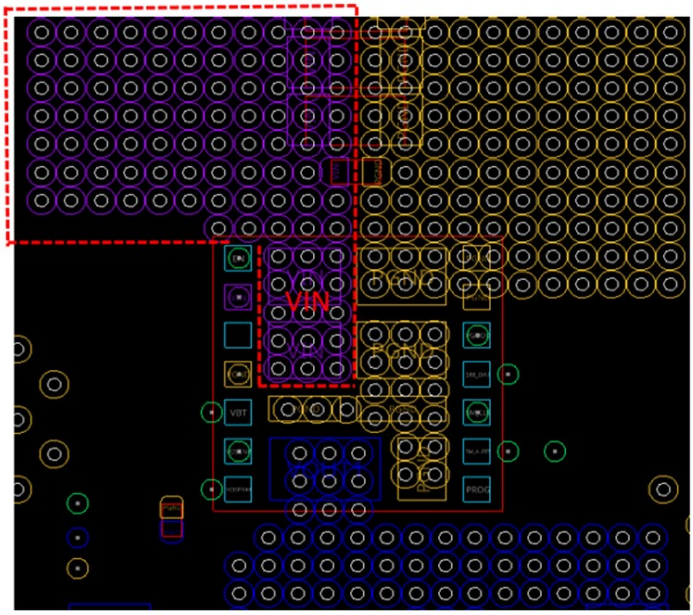
The evaluation board layout and schematic files are available for interested users. These can be downloaded through the webpage or by contacting our Field Applications Engineer through the help section of the webpage. The electrical and the thermal characterization of the FPLX030A0XY3-SRZ module has been done on evaluation boards with layout shown in figure below.



Example of Pad Layout with Vias.

Layout guidelines are provided based on the full rated FPLX030. Following are the recommendations for this converter.

1. For Thermal and Current Carrying reasons, it is recommended to have six 20 mil heavy plated filled vias on Vin, Vout and bigger ground pads as shown in figure below. Copper plating of vias should be 2 mils if possible.
2. 12 mil vias are recommended for all Signal Pins
3. Additional thermal vias can be placed around module near ground plane, Vin and Vout pad to transfer heat.

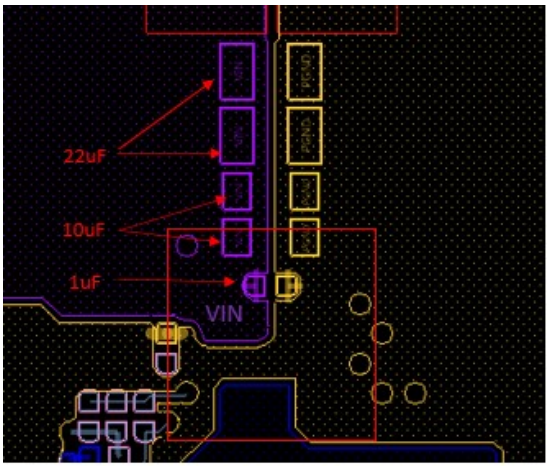


Example of Pad Layout with Vias.

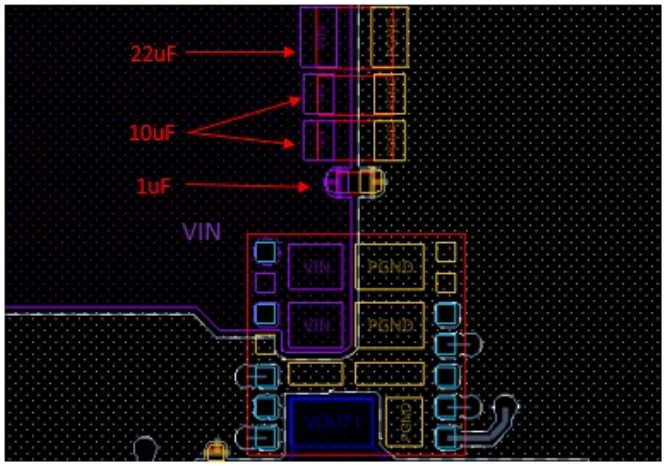
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Layout considerations (continued)

In bottom side of the customer board place a minimum of 10 µf and 1 µf input capacitor directly under V_{IN} [see figure below left] and keep additional input capacitance as close as possible to the Vin of the module [see figure below right].

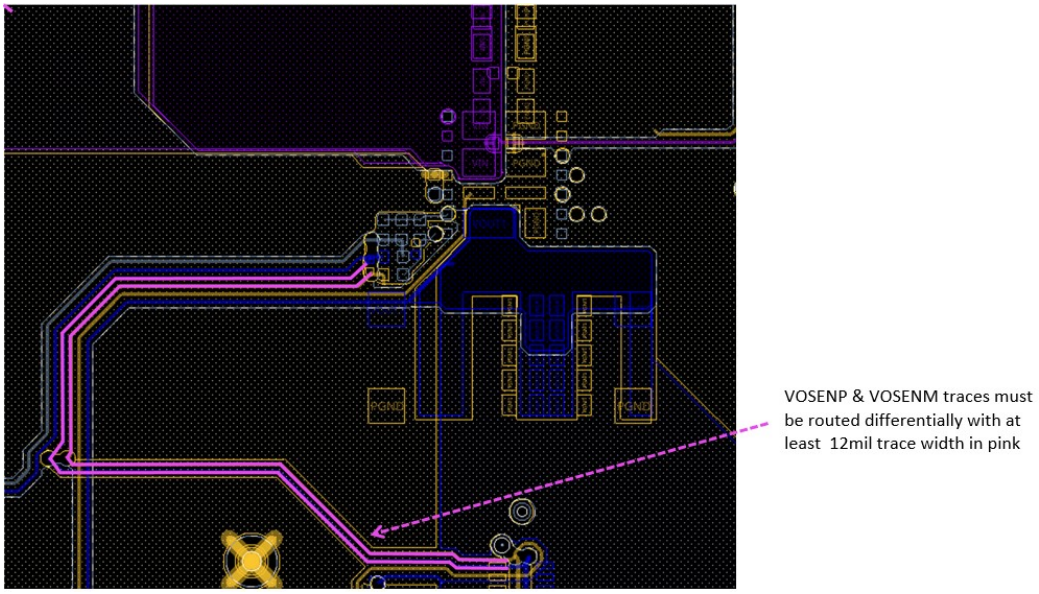


1uF & 10uF Capacitor under V_{IN}Pad



More Capacitors on top surface close to V_{IN} Pad

Remote sense traces must be routed differentially with at least 12 mil trace width. running close each other and away from any noise source or high current power plane, shield the pair of remote sensing lines with ground planes above and below [see figure below]

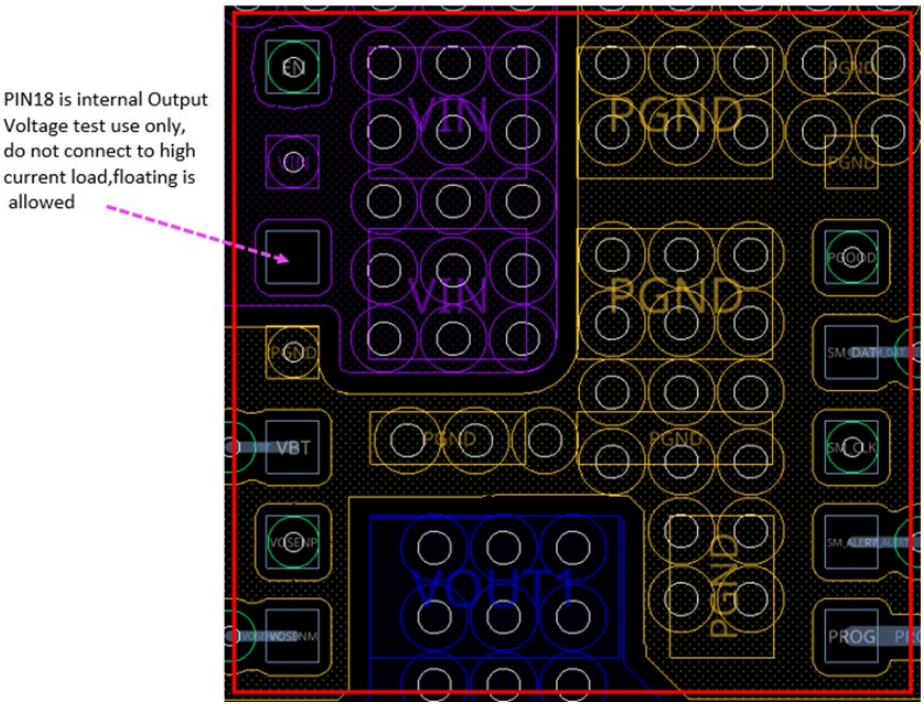


Remote Output Voltage Sense-VOSENP & VOSENM Traces

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Layout considerations (continued)

Pin18 of module is used for internal test only, do not connect to high current load due to limited current capability. Floating is allowed [see figure below].



Unconnected pad to PIN18 of module

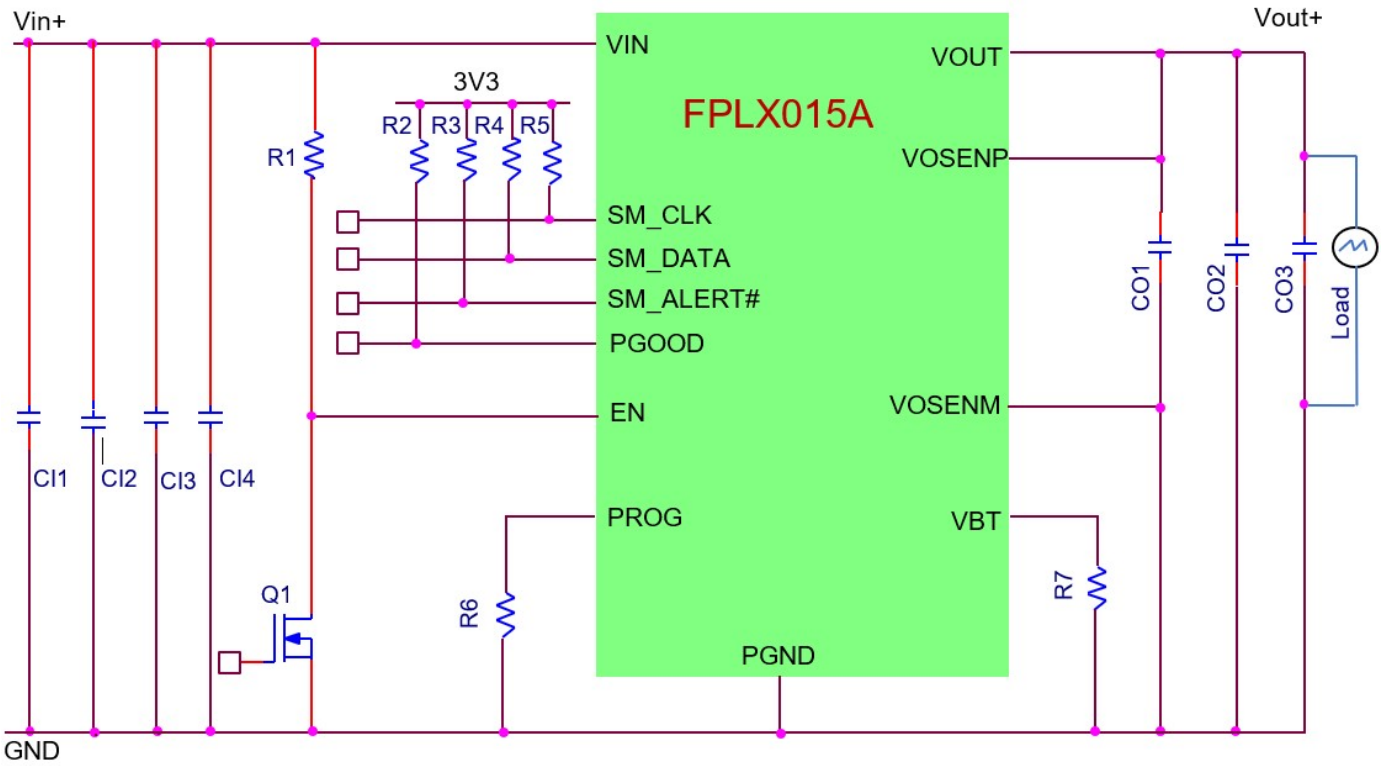
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Application Circuit (Based on Evaluation Board)

Without feedback resistor divider

V_{IN} = 12 V_{DC}

V_{out} = 0.45—2.0 V_{DC}



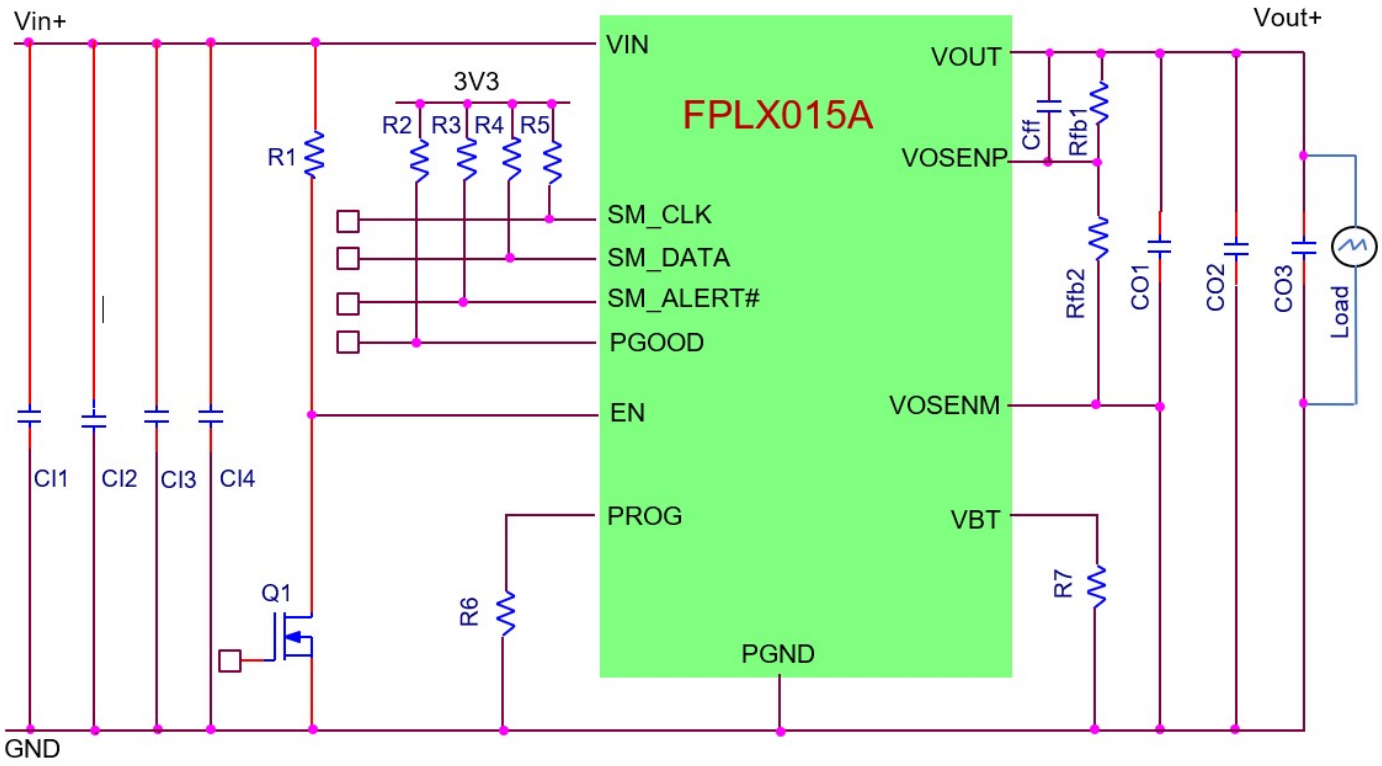
CI4 – Banks (2 x 1 µF ceramic)
CI3 – Banks (4 x 10 µF ceramic)
CI2 – Banks (4 x 22 µF ceramic)
CI1 – Banks (1 x 560 µF electrolytic)
CO1 – 6 x 0.047 µF+ 8 x 0.1 µF - ceramic
CO2 – 2 x 22 µF ceramic + 20 x 47 µF ceramic +2x470 µF polymer or electrolytic
CO3 – 1 x 1500 pF (0402) + 1 x 2200 pF (0402) +1 x 0.022 µF (0402) + 0.1 uF (0402) – all ceramic
R1 based on Q1
R2, R3, R4, R5 = 10 kΩ (Default)
R3, R4, R5 – based on PMBus controller / dongle being used
R6= 0Ω (Default) - See PMBus addressing section
R7= 0Ω (Default) – See “Setting output voltage with external resistor” –section
3.3V must be provided externally
EN pin must not be left floating
VBT pin must not be left floating

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Application Circuit (Based on Evaluation Board)

With feedback resistor divider

V_{IN} = 12 V_{DC}
V_{out} = 2.0 – 3.6 V_{DC}
V_{out} = 0.5 – 2.0 V_{DC} (not recommended, but can also be used for ≤2.0V with lower setpoint accuracy)

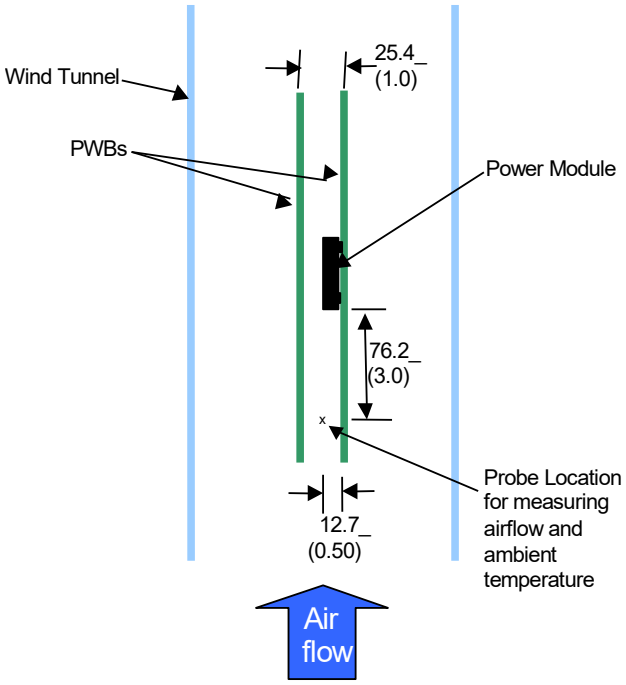


CI4 – banks (2 x 1 µF ceramic)
CI3 – Banks (4 x 10 µF ceramic)
CI2 – Banks (4 x 22 µF ceramic)
CI1 – Banks (1 x 560 µF electrolytic)
CO1 – 6 x 0.047 µF+ 8 x 0.1 µF - ceramic
CO2 – 2 x 22 µFceramic + 20 x 47 µF ceramic +2x470 µF polymer or electrolytic
CO3 – 1 x 1500 pF (0402) + 1 x 2200 pF (0402) +1 x 0.022 µF (0402) + 0.1 uF (0402) – all ceramic
R1 based on Q1
R2, R3, R4, R5 = 10 kΩ (Default)
R3, R4, R5 – based on PMBus controller / dongle being used
R6= 0Ω (Default) - See PMBus addressing section
R7= 0Ω (Default) – See Output voltage setting by VBT pin strap resistor
Rfb1, Rfb2 = 499 Ω
Cff – feedforward capacitor to reduce jitter
3.3V must be provided externally
EN pin must not be left floating
VBT pin must not be left floating

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Thermal Considerations

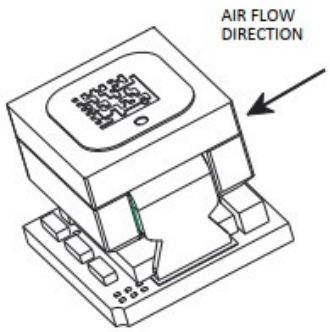
Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation. Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented



Thermal test setup

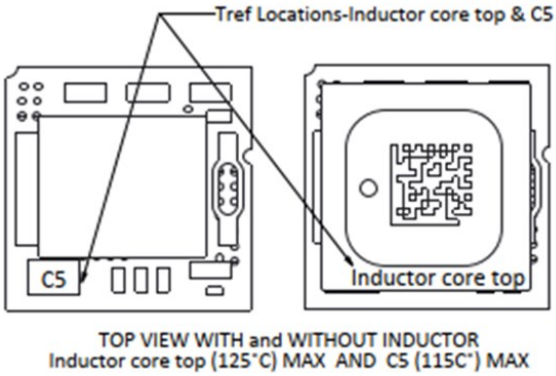
here is based on physical measurements taken in a wind tunnel. The test set-up is shown below.

The preferred airflow direction for cooling the module is shown below.



Preferred airflow direction

The thermal reference points, Tref used in the specifications are shown below. For reliable operation the temperatures at these points should not exceed 125°C (inductor core top) and 115°C (C5). The output power of the module should not exceed the rated power of the module (Vo,set x Io,max).



Location of the thermal reference points (Tref)

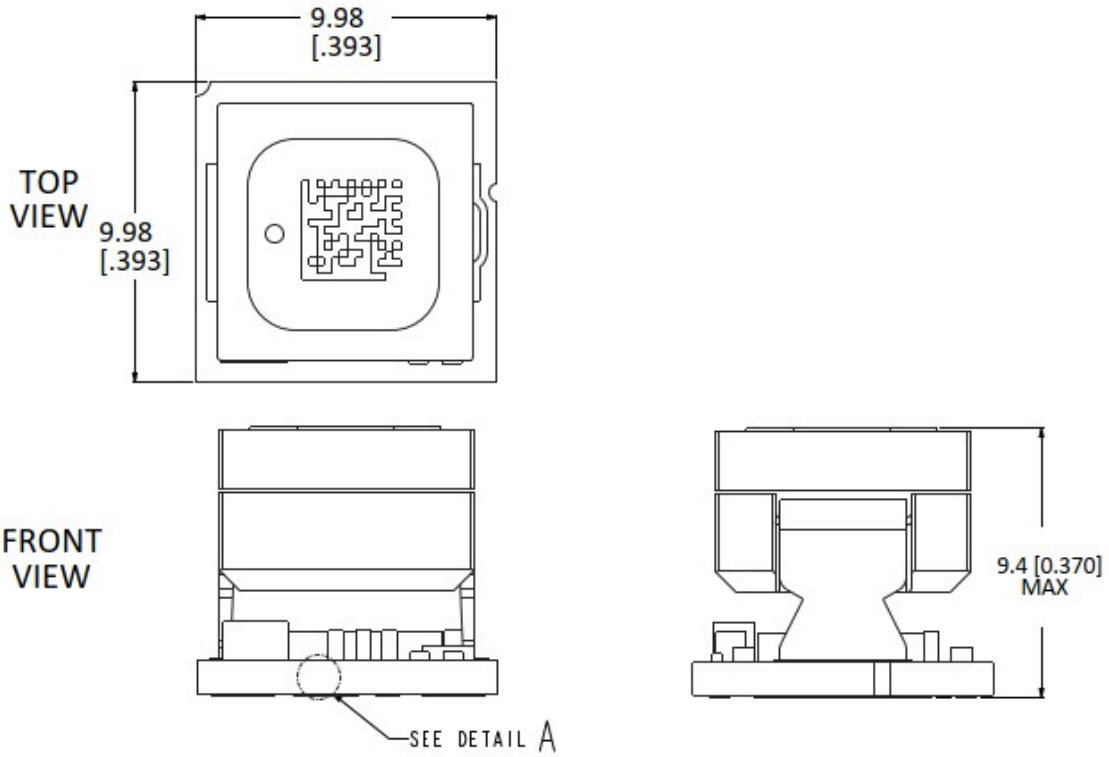
Please refer to the Application Note “Thermal Characterization Process for Open-Frame Board-Mounted Power Modules” for a detailed discussion of thermal aspects including maximum device temperatures. Increased airflow over the module enhances the heat transfer via convection. The thermal derating in Characteristic Curves section show the maximum output current that can be delivered by each module in the indicated orientation without exceeding the maximum Tref temperature versus local ambient temperature (TA) for several air flow conditions. The thermal derating curves were generated using a 8 layer evaluation board with 2 oz copper inner layers and 2 oz in outer layers.

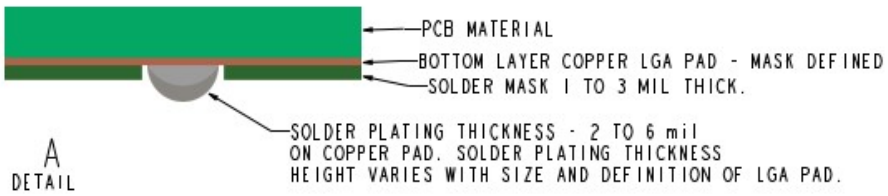
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Mechanical Outline

Dimensions are in millimeters and (inches).

Tolerances: x.x mm ± 0.5mm (x.xx in. ±0.02 in.) [unless otherwise indicated]
x.xx mm ± 0.25 mm (x.xxx in ±0.010 in.)





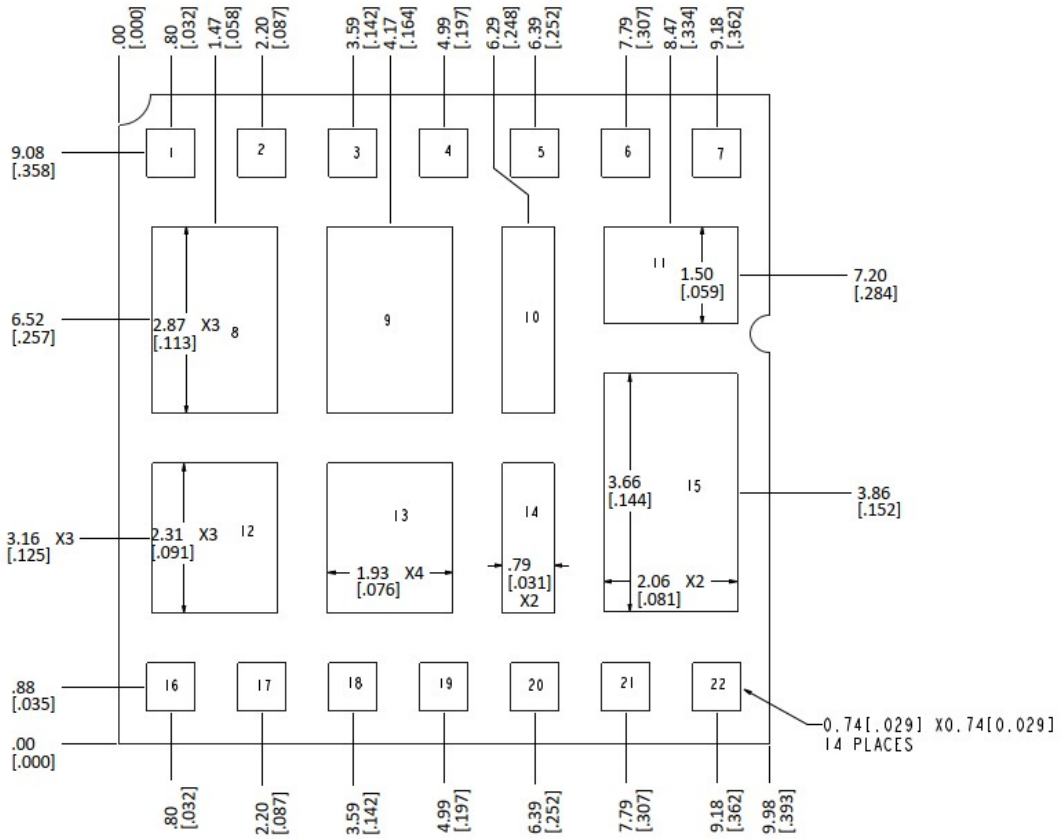
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Recommended Pad Layout

Dimensions are in millimeters and (inches).

Tolerances: x.x mm ± 0.5mm (x.xx in. ±0.02 in.) [unless otherwise indicated]

x.xx mm ± 0.25 mm (x.xxx in ±0.010 in.)



PIN	FUNCTION
1	PGND
2	PGND
3	PGOOD
4	SM_DATA
5	SM_CLK
6	SM_Alert
7	PROG
8	PGND
9	PGND
10	PGND
11	PGND
12	VIN
13	VIN
14	PGND
15	VOUT
16	EN
17	VIN
18	VOUT
19	PGND
20	VBT
21	VOSENP
22	VOSENM

V_{IN} pin 17 and V_{OUT} pin 18 are for OmniOn Power manufacturing testing and cannot handle high current. Connecting to pins 17 and 18 is optional. They are internally connected.

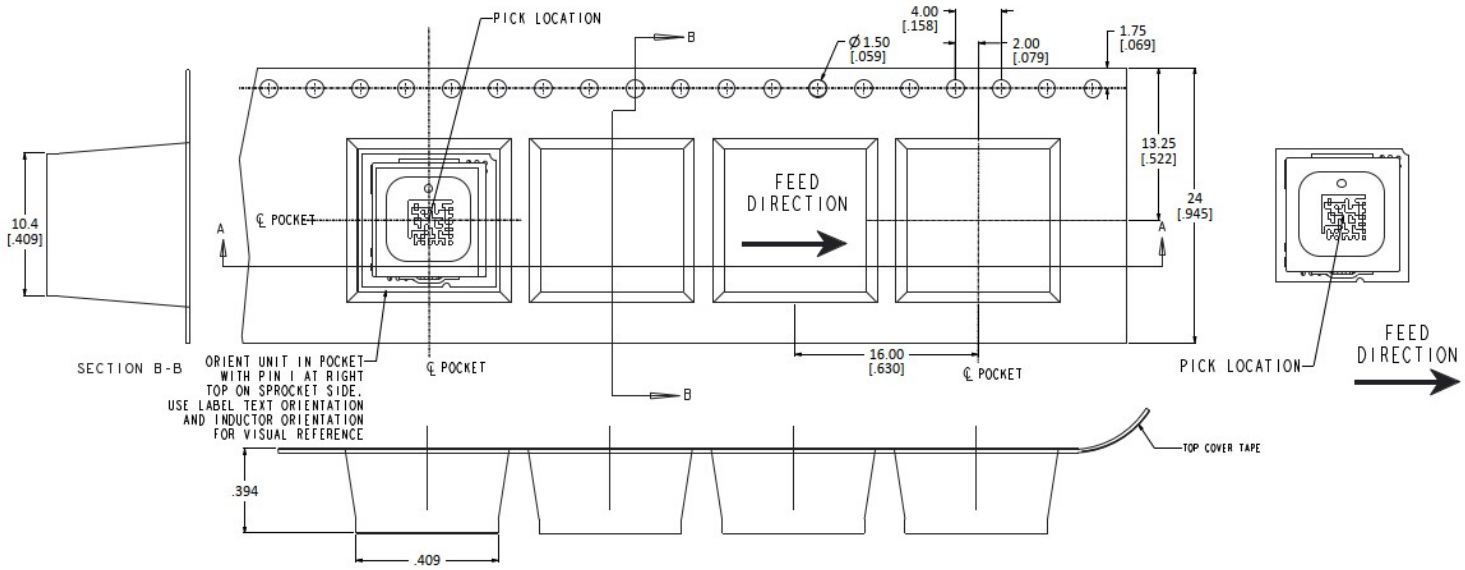
EN and VBT pins must not be left floating.

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Packaging Details

Digital FemtoPlus DLynx III ™ modules are supplied in tape & reel as standard. Modules are shipped in quantities of 250 modules per reel.

All Dimensions are in millimeters and (in inches).



Reel dimensions

Outside dimensions:	330.2 mm (13.00 inches)
Inside dimensions:	177.8 mm (7.00 inches)
Tape width:	24.0 mm (0.945 inches)

Packing length per 13 inch reel is 3.9 meters.

Pocket position relative to sprocket hole is measured as true position of pocket, not pocket hole.

Camber in compliance with EIA 481

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Pick and Place

The FPLX015 Open Frame modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards. The label also carries product information such as product code, serial number, manufacturing week and the location of manufacture.

Nozzle and Stencil Recommendations

The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3 mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7 mm.

Solder volume is critical for reliable production process. Below tables show the suggested stencil size for each pad type based on 5 mil stencil thickness of customer board.

PIN #	Function	Stencil opening (mils)
1	PGND	25 x 25
2	PGND	25 x 25
3	PGOOD	25 x 25
4	SM_DATA	25 x 25
5	SM_CLK	25 x 25
6	SM_Alert	25 x 25
7	PROG	25 x 25
8	PGND	71 x 109
9	PGND	71 x 109
10	PGND	26 x 109
11	PGND	55 X 77

PIN #	Function	Stencil opening (mils)
12	VIN	71 x 87
13	VIN	71 x 87
14	PGND	26 x 85
15	VOUT	77 x 139
16	EN	25 x 25
17	VIN	25 x 25
18	VOUT	25 x 25
19	PGND	25 x 25
20	VBT	25 x 25
21	VOSENP	25 x 25
22	VOSENM	25 x 25

Bottom Side / First Side Assembly

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

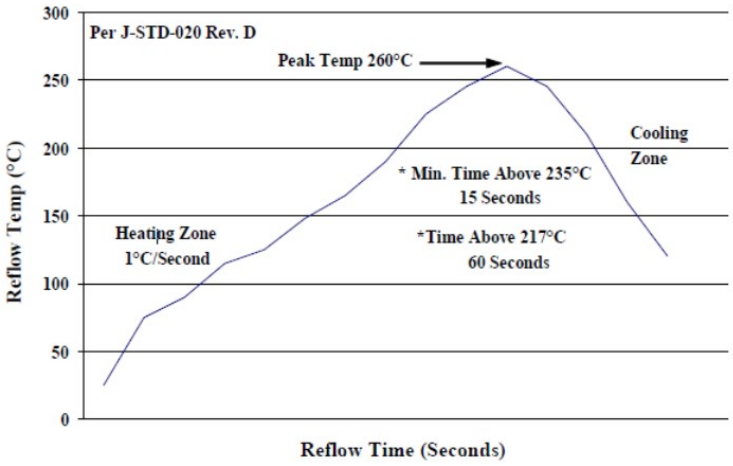
Lead Free Soldering

The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

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Pb-free Reflow Profile

Power Systems will comply with J-STD-020 Rev. D (Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package. The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended linear reflow profile using Sn/Ag/Cu solder is shown in below. Soldering outside of the recommended profile requires testing to verify results and performance.



Recommended linear reflow profile using Sn/Ag/Cu solder

MSL Rating

The FPLX030A0XY3-SRZ Open Frame modules have a MSL rating of 2A.

Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of 30°C and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40°C, < 90% relative humidity.

Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to Board Mounted Power Modules: Soldering and Cleaning Application Note (AN04-001).

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Ordering Information

Please contact our Sales Representative for pricing, availability, and optional features.

Table 5. Device Codes

Device Code	Input Voltage Range	Output Voltage	Output Current	On/Off Logic	Ordering code
FPLX015A0XY3-SRZ	6 – 14V_{DC}	0.45 – 3.6 V_{DC}	15A	Programmable	1600482260A

Table 6. Coding Scheme

Module type Identifier	Family	Sequencing Option	Output current	Output voltage	On/Off logic	Remote Sense	Options	ROHS Compliance
FP	L	X	015A0	X	Y	3	-SR	Z
FP=FemtoPlus	L = DLynx III	X=digital sequencing only , no analog sequencing pin	15A	X = programmable output	Y = programmable enable logic	3 = Remote Sense	S = Surface Mount R = Tape & Reel	Z = ROHS Compliant

Table 7 Orderable Accessories

Manufacturer Part Number	Ordering Code	Description
EVAL FPLX015A0XY3-SRZ	1600482259A	Evaluation Board with FPLX015 module
I2C_USB_DONGLE_2.X_WITH_CABLES_AND_POL_EVAL_BOARD	CC109164430	Digital Power Insights (DPI) kit with USB dongle, needed cables, and a digital POL evaluation board (PDT012 or PJT020) and quick guide
I2C_USB_DONGLE_2.X_WITH_CABLES	150036482	USB dongle and cables required for use of Digital Power Insights software. Evaluation board is not included.
I2C_USB_DONGLE_2.x	1600218857A	USB dongle required for use of Digital Power Insights software. Cables or evaluation board are not included

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Change History (excludes grammar & clarifications)

Revision	Date	Description of the change
1.0	6/14/2024	Initial release
1.1	2/7/2025	Capacitor Updates
1.2	3/3/12025	Updated transient curve and quick start
1.3	4/14/2025	Updated quick start section
1.4	05/12/2025	Update External Capacitance data on Pg. 4
1.5	12/2/2025	Clarifications in quick start guide for VBT+PMBus mode.

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OmniOn Power Inc.

601 Shiloh Rd.

Plano, TX USA

omnionpower.com

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