ATXW150: Non-Isolated DC-DC Power Modules

$5V_{dc}$ – $59V_{dc}$ Input; $2V_{dc}$ to $30V_{dc}$ Output; 15A to 5A Scaled output, 150W Max

RoHS Compliant

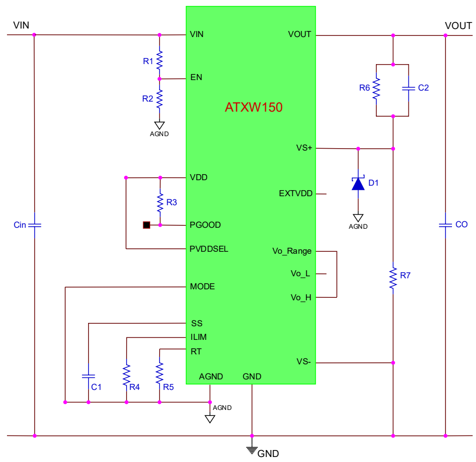
Quick Start Process

1. Keep EN pulled low to ensure module is off (skip this step if using resistor divider for EN).
2. Check that desired target output voltage setting is set by selecting a Rtrim value based on equation 1.
3. Check that Vo_Range and RT are configured correctly, based on if target output is V_{OUT} > 14V or V_{OUT} ≤ 14V.
4. Check if PVDDSEL is configured correctly based on if input voltage is V_{IN} > 14V or V_{IN} ≤ 14V.
5. Apply input power. If using resistor divider on EN pin, module will begin to provide output once input voltage is detected.
6. If not using resistor divider on EN, pull EN high to enable module.

Applications

- Industrial equipment
- Distributed power architectures
- Intermediate bus voltage applications
- Telecommunications equipment

Application Schematic – Typical



Features

- Compliant to RoHS Directive 2011/65/EU and amended Directive (EU) 2015/863
- Compliant to REACH Directive (EC) No 1907/2006
- Compatible in a Pb-free or SnPb reflow environment
- Compliant to IPC-9592B (Nov. 2012), Class II
- Buck Converter Operation Mode
- Positive logic remote On/Off
- Output over current protection (non-latching)
- Differential Remote Sense
- Monotonic Startup
- Small size and low profile:
  29.7 mm x 16 mm x 14.5 mm (max).
  (1.17 in x 0.63 in x 0.57 in (max).
- Output voltage programmable from 2 V_{dc} to $30V_{dc}$ via external resistor (Step-Down only).
- Wide operating temperature range (-40°C to 105°C)
- ANSI/UL* 62368-1 and CAN/CSA† C22.2 No. 62368-1, DIN VDE‡ 0868-1/A11:2017 (EN62368- 1:2014/A11:2017), PENDING
- ISO** 9001 and ISO 14001 certified manufacturing facilities.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Parameter	Device	Symbol	Min	Max	Unit
Input Voltage Continuous	All	V_{IN}	-0.3	59	V_{dc}
Operating Ambient Temperature (see Thermal Considerations section)	All	T_A	-40	105	°C
Storage Temperature	All	T_{stg}	-55	125	°C
Enable Pin			-0.3	V_{IN} + 0.3	V
VDD to AGND			-0.3	6	V
Vo_Range, Vo_L, Vo_H to PGND			-0.3	V_{IN} + 0.3	V
PVDDSEL, MODE, RT, ILIM, SS, PG to AGND			-0.3	6.3	V

Electrical Specifications

Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions (-40 to 85°C).

Parameter	Device	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	All	V_{IN}	5	-	59	V_{dc}
Maximum Input Current (V_{IN}=5 to 59V, I_O=$I_{O, max}$)	All	$I_{IN, max}$			12	A_{dc}
Input No Load Current (V_{IN} = 24/36/48V, I_O = 0, module enabled)	$V_{O, set}$ = 3.3/ 5/ 9/ 12/ 18V_{dc}	$I_{IN, No load}$			35/ 42/ 60/ 76/105	mA
(V_{IN} = 36/48, I_O = 0, module enabled)	$V_{O, set}$ = 24 / 28V_{dc}	$I_{IN, No load}$			285/ 144	mA
Input Stand-by Current, (module disabled) V_{IN} = 24 V_{dc}, V_{IN} = 28 V_{dc}, V_{IN} = 32 V_{dc}, V_{IN} = 36 V_{dc}, V_{IN} = 48 V_{dc},	All	$I_{IN, stand-by}$			1.5 1.6 1.6 1.8 1.3	mA
Inrush Transient	All	I^2t	-	-	4.6	A^2s
Input Terminal Ripple Current, (5Hz to 20MHz, 12μH source impedance; V_{OUT} = 3.3V, I_O = $I_{O, max}$; see Test Configurations)	All		-	0.8	-	A_{p-p}
V_{OUT} =12V, I_O=$I_{O, max}$				1.8		A_{p-p}
V_{OUT} =28V, I_O=$I_{O, max}$				2.1		A_{p-p}
Input Ripple Rejection (120Hz)	All		-	-	-39	dB

CAUTION: This power module is not internally fused. An input line fuse must always be used. See safety section in this DS for value.

Electrical Specifications (continued)

Parameter	Device	Symbol	Min	Typ	Max	Unit
Output Voltage Set-point Accuracy -40°C to 85°C, V_o=3.3 to 28V (0.1% resistor w/ TC 100ppm required)	All	$V_{o, set}$		±1		$\%V_{O, set}$
Output Voltage Set-point	All	V_{OUT}	2		30	V_{dc}
Output Voltage Line Regulation (V_{IN} = $V_{IN, min}$ to $V_{IN, max}$ and I_O = $I_{O, max}$) V_O=3.3/ 5/ 9/ 12 V_O=18/ 24/ 28	 All All			 0.2/0.2/0.2/0.6 0.5/0.4/0.5		$\%V_{O, set}$
Output Load Regulation, V_{IN}=48V Load (I_O = $I_{O, min}$ to $I_{O, max}$) V_O=3.3/ 5/ 9/ 12 V_O=18/ 24/ 28	 All All				 0.13/0.16/0.20/0.21 0.06/0.07/0.054	$\%V_{O, set}$
Remote Sense Range	All			0.3		V_{dc}
Input Noise, nominal output, (V_{IN} = $V_{IN, nom}$ and I_O=$I_{O, min}$ to $I_{O, max}$, C_{IN} = 1x0.1µF, 5x10uF ceramic capacitors and 220uF (electrolytic), 25°C Ambient, 500MHz BW	All			2		$\%V_{IN}$
Output Ripple and Noise on nominal output (V_{IN} = $V_{IN, nom}$ and I_O=$I_{O, min}$ to $I_{O, max}$ C_O = 1x0.1µF, 6x1uF, 10x10uF ceramic capacitors and 220uF (electrolytic), C_{IN} = 1x0.1µF, 5x10uF ceramic capacitors and 220uF (electrolytic), 25°C Ambient, 20MHz BW	All			2.5		$\%V_O$
Output Ripple and Noise on nominal output (V_{IN} = $V_{IN, nom}$ and I_O = $I_{O, min}$ to $I_{O, max}$ capacitors as above row)						
V_O =3.3V, V_{IN}=24V Peak-to-Peak (5Hz to 20MHz bandwidth) RMS (5Hz to 20MHz bandwidth)	 All All			 25 6		 mV_{pk-pk} mV_{rms}
V_O=5V, V_{IN}=24V Peak-to-Peak (5Hz to 20MHz bandwidth) RMS (5Hz to 20MHz bandwidth)	 All All			 33 9		 mV_{pk-pk} mV_{rms}
V_O=12V, V_{IN}=24V Peak-to-Peak (5Hz to 20MHz bandwidth) RMS (5Hz to 20MHz bandwidth)	 All All			 49 14		 mV_{pk-pk} mV_{rms}
V_O=28V, V_{IN}=48V Peak-to-Peak (5Hz to 20MHz bandwidth) RMS (5Hz to 20MHz bandwidth)	 All All			 68 21		 mV_{pk-pk} mV_{rms}
External Capacitance	All	$C_{O, max}$			1x220+10x10+1x0.1 (50V rated)	µF
Output Current V_O=3.3V V_O=12V V_O=18V V_O=28V	All	 I_O I_O I_O I_O			 15 15 8.3 5.36	 A_{dc} A_{dc} A_{dc} A_{dc}

Electrical Specifications (continued)

Parameter	Device	Symbol	Min	Typ	Max	Unit
Output Current Limit Inception (Hiccup Mode) (current limit does not operate in sink mode), V_{IN} = 24V, V_{OUT} = 3.3V V_{IN} = 24V, V_{OUT} = 5V V_{IN} = 24V, V_{OUT} = 9V V_{IN} = 24V, V_{OUT} = 12V V_{IN} = 24V, V_{OUT} = 18V V_{IN} = 36V, V_{OUT}= 24V V_{IN} = 36V, V_{OUT}= 28V					 19.8 19.3 19.1 19 14.8 12.8 12	 A_{dc} A_{dc} A_{dc} A_{dc} A_{dc} A_{dc} A_{dc}
Efficiency (I_O=$I_{O, max,}$) V_{IN} = 24V_{dc}, T_A=25°C V_{IN} = 24V_{dc}, T_A=25°C V_{IN} = 24V_{dc}, T_A=25°C V_{IN} = 48V_{dc}, T_A=25°C	 $V_{o, set}$ = 3.3V_{dc} $V_{o, set}$ = 5V_{dc} $V_{o, set}$ = 12V_{dc} $V_{o, set}$ = 28V_{dc}	 η η η η		 90.9 93.9 96.7 95.4		 % % % %
Switching Frequency	All	f_{sw}		200	—	kHz

General Specifications

Parameter	Min	Typ	Max	Unit
Calculated MTBF (I_O=0.8$I_{O, max}$, T_A=40°C) Telcordia Issue 2, Method 1 Case 3		>7,000,000		Hours
Weight	—	17 (0.599)	—	g (oz.)

Feature Specifications

Parameter	Device	Symbol	Min	Typ	Max	Unit
On/Off Signal Interface (V_{IN}=$V_{IN, min}$ to $V_{IN, max}$; open collector or equivalent, Signal referenced to GND) Device Code with suffix "4" – Positive Logic (See Ordering Information)						
Logic High (Module ON) Input High Current Input High Voltage	All	IIH VIH	— 1.12	— 1.2	0.1 1.32	μA V_{dc}
Logic Low (Module OFF) Input low Current Input low Voltage	All	IIL VIL	— -0.3	— —	0.03 1.1	μA V_{dc}
Turn-On Delay and Rise Times (V_{IN}=$V_{IN, nom}$, I_O=$I_{O, max}$, V_O=$V_{O, nom}$, to within ±1% of steady state)						
Input power is applied for at least one second and then the On/Off input is enabled (delay from instant at which Von/Off is enabled until V_o=10% of $V_{o, set}$)	All	T_{delay}	—	4	—	msec
Output voltage Rise time (time for V_o to rise from 10% of $V_{o, set}$ to 90% of $V_{o, set}$)	All	T_{rise}	—	12	—	msec
Output voltage overshoot (T_A=25°C, V_{IN}=$V_{IN, min}$ to $V_{IN, max}$, and I_O=$I_{O, min}$ to $I_{O, max}$) With or without maximum external capacitance				1		$\%V_{O, set}$
Over Temperature Protection (See Thermal Considerations section)	All	T_{ref}			125	°C
Input Undervoltage Lockout at V_{IN}=5V and V_{OUT}=3.3 V Turn-on Threshold Turn-off Threshold	All All		3.55 3.35	4.2	4.8 4.5	V_{dc}

Characteristic Curves

The following figures provide typical characteristics for the 5-59V ProLynx2 15A at $3.3V_{OUT}$ and at 25°C.

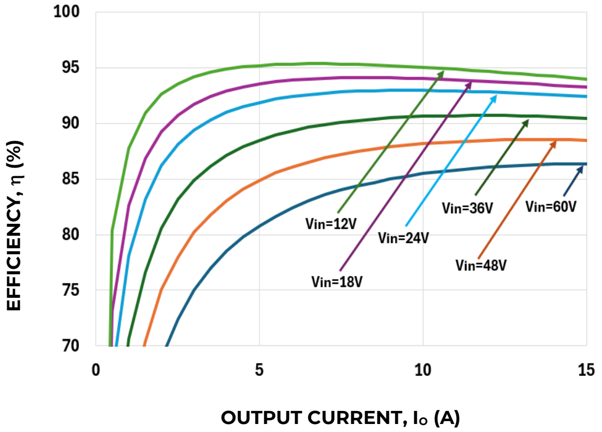


Figure 1. Converter Efficiency versus Output Current.

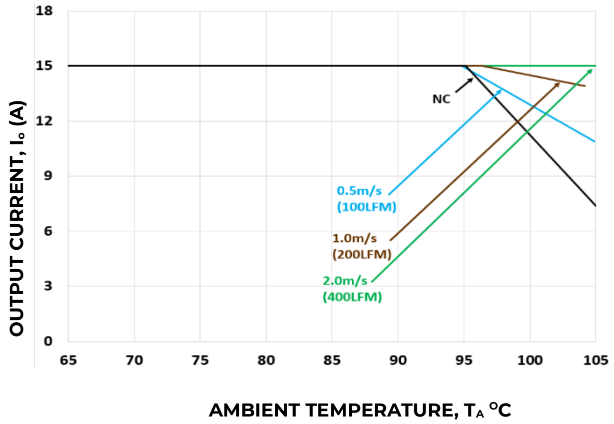


Figure 2. Converter Output versus Ambient Temperature, $28V_{IN}$.

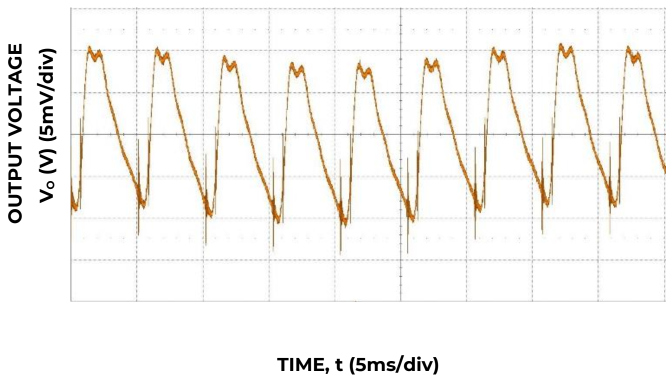


Figure 3. Typical Output Ripple at $24V_{IN}$, $I_{O\,max}$, and C_O = 1x0.1µF, 6x1uF, 10x10uF (Ceramics) and 220uF (electrolytic).

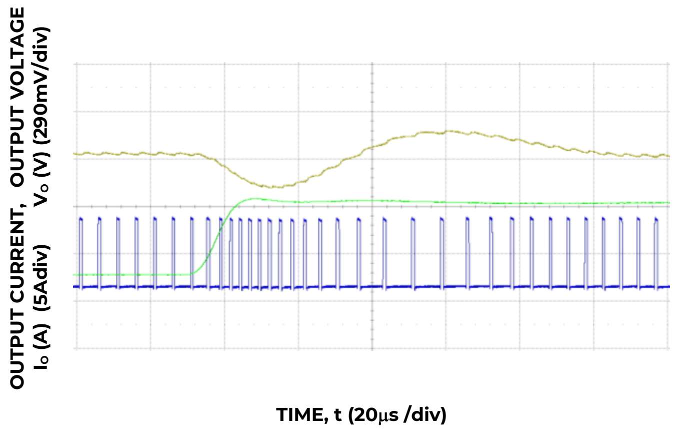


Figure 4. Transient Response to Dynamic Load Change from 50% to 100% at $24V_{IN}$, C_O = 1x0.1µF, 6x1uF, 10x10Uf (Ceramics) and 220uF (electrolytic).

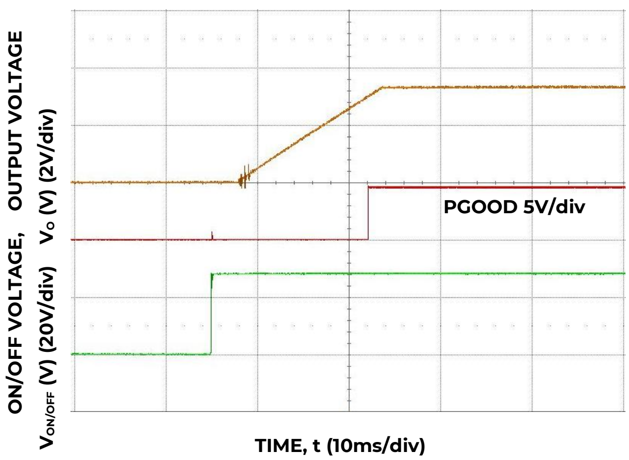


Figure 5. Typical Start-up Using On/Off Voltage (V_{IN} = 28V, $I_{O,\,max}$).

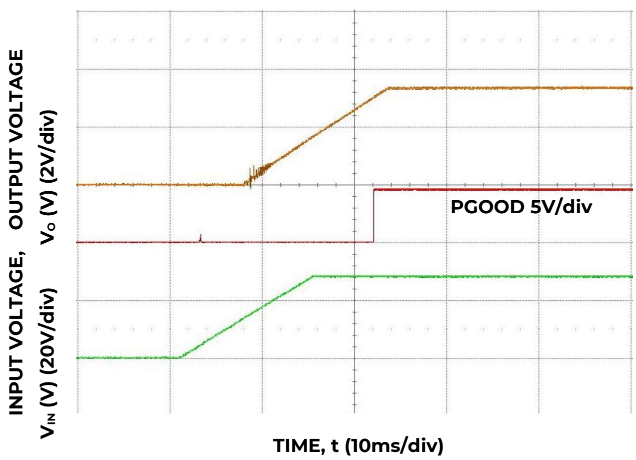


Figure 6. Typical Start-up Using Input Voltage (V_{IN} = 28V, $I_{O,\,max}$).

Characteristic Curves (continued)

The following figures provide typical characteristics for the 5-59V ProLynx2 15A at $5V_{OUT}$ and at 25°C.

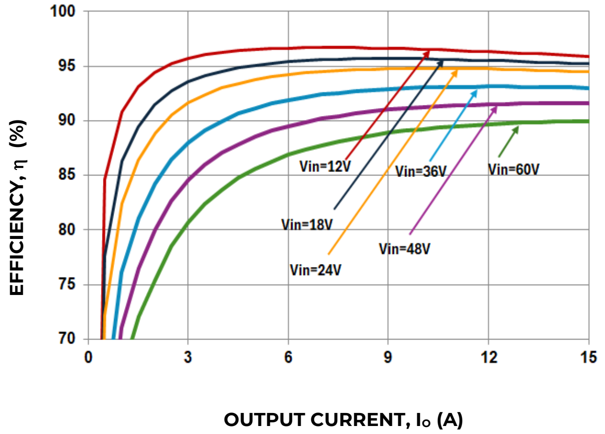


Figure 7. Converter Efficiency versus Output Current.

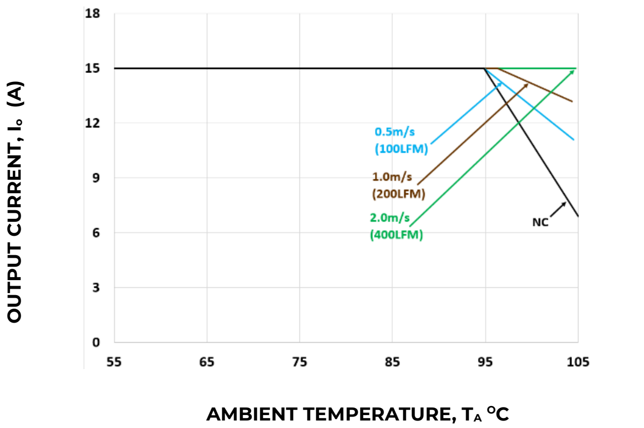


Figure 8. Converter Output versus Ambient Temperature, $28V_{IN}$.

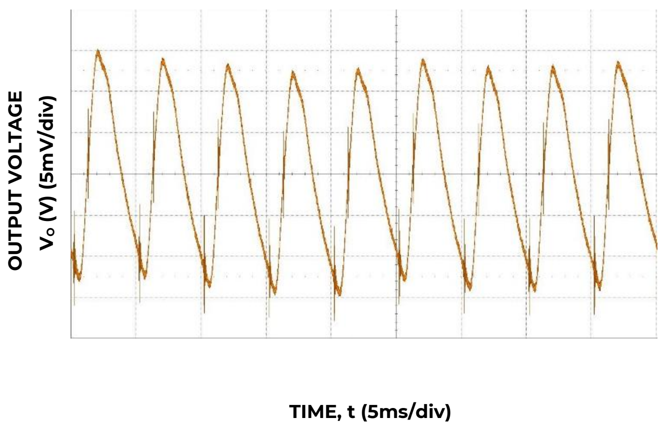


Figure 9. Typical Output Ripple at 24V Input, $I_{O,\,max}$ and C_O = 1x0.1μF, 6x1uF, 10x10uF (ceramics) and 220uF (electrolytic).

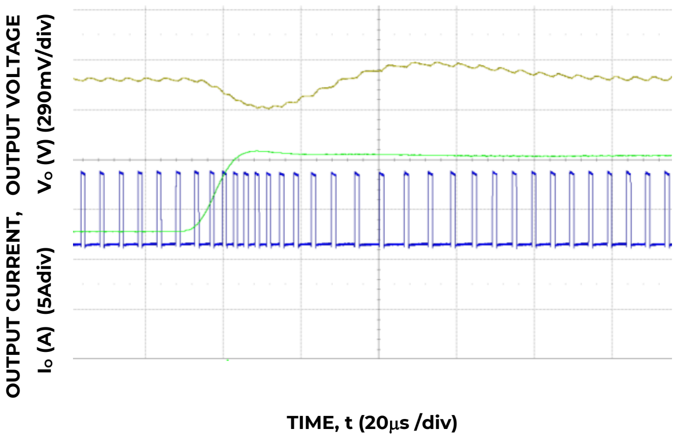


Figure 10. Transient Response to Dynamic Load Change from 50% to 100% at $24V_{IN}$, C_O = 1x0.1μF, 6x1uF, 10x10uF (ceramics) and 220uF(electrolytic).

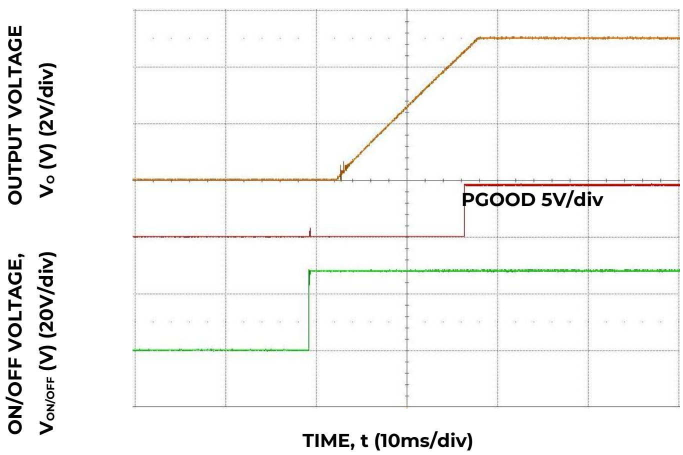


Figure 11. Typical Start-up Using On/Off Voltage (V_{IN} = 28V, $I_{O,\,max}$).

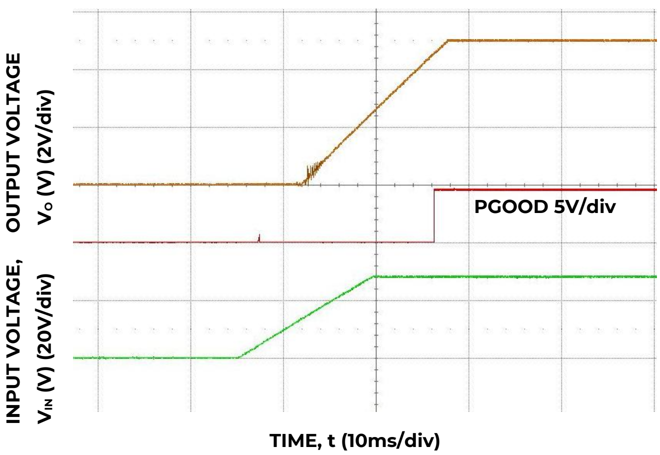


Figure 12. Typical Start-up Using Input Voltage (V_{IN} = 28V, $I_{O,\,max}$).

Characteristic Curves (continued)

The following figures provide typical characteristics for the 5-59V ProLynx2 15A at 12 V_{OUT} and at 25°C

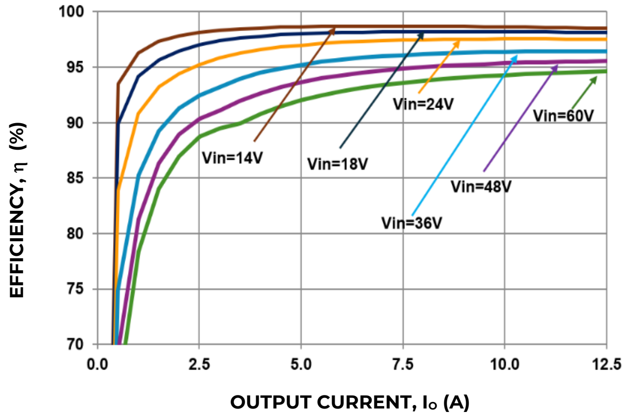


Figure 13. Converter Efficiency versus Output Current.

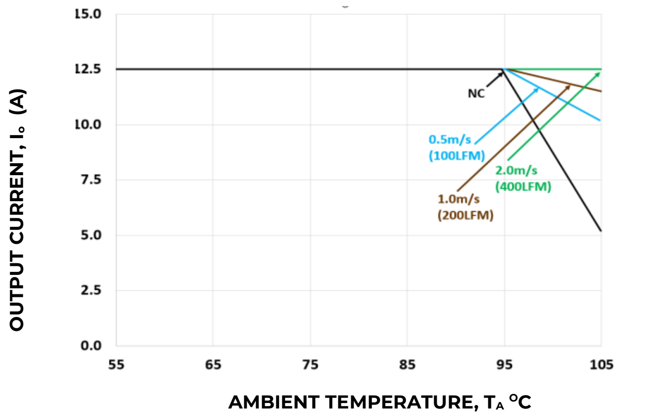


Figure 14. Converter Output versus Ambient Temperature, 28V_{IN}.

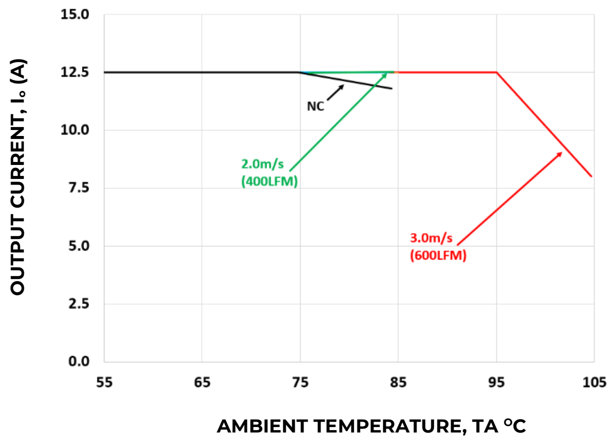


Figure 15. Converter Output versus Ambient Temperature, 48V_{IN}.

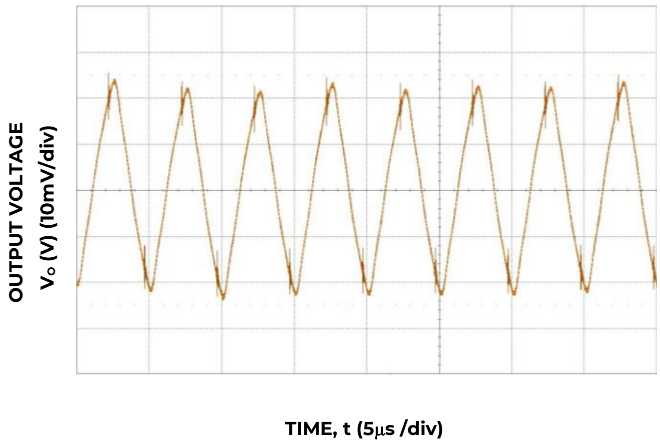


Figure 16. Typical Output Ripple at 24V Input, $I_{O,\,max}$ and C_O = 1x0.1µF, 6x1uF, 10x10uF (ceramics) and 220uF (electrolytic).

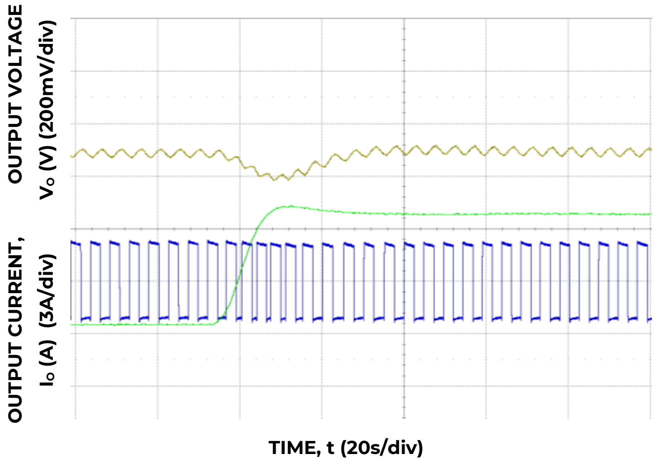


Figure 17. Transient Response to Dynamic Load Change from 50% to 100% at 24V_{IN}, C_O = 1x0.1µF, 6x1uF, 10x10uF (ceramics) and 220uF(electrolytic).

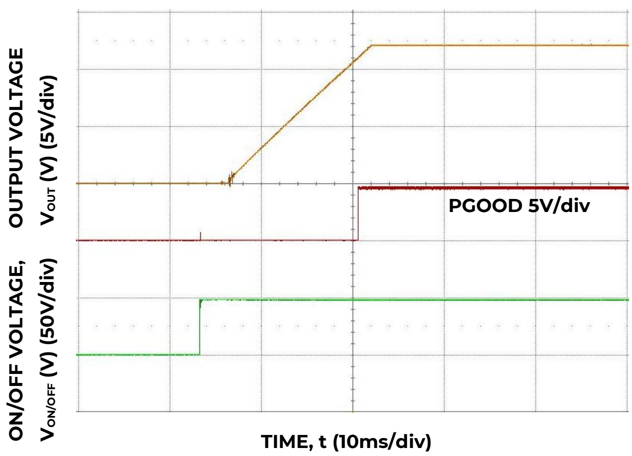


Figure 18. Typical Start-up Using On/Off Voltage (V_{IN} = 48V, $I_{O,\,max}$).

Characteristic Curves (continued)

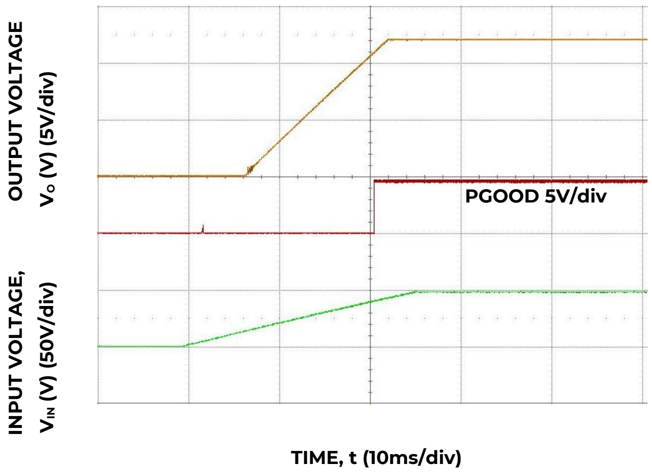


Figure 19. Typical Start-up Using Input Voltage (V_{IN} = 48V, $I_{O,\ max}$).

Characteristic Curves (continued)

The following figures provide typical characteristics for the 5-59V ProLynx2 15A at 28 V_{OUT} and at 25°C

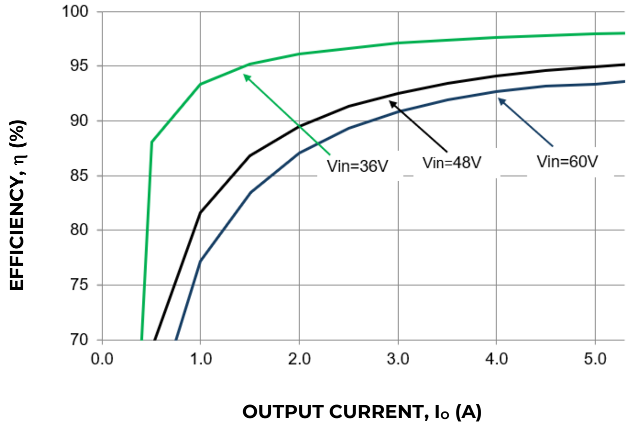


Figure 20. Converter Efficiency versus Output Current.

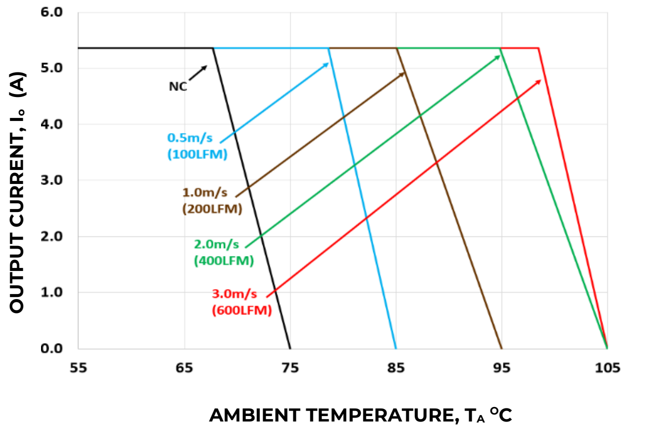


Figure 21. Converter Output versus Ambient Temperature, 48V_{IN}.

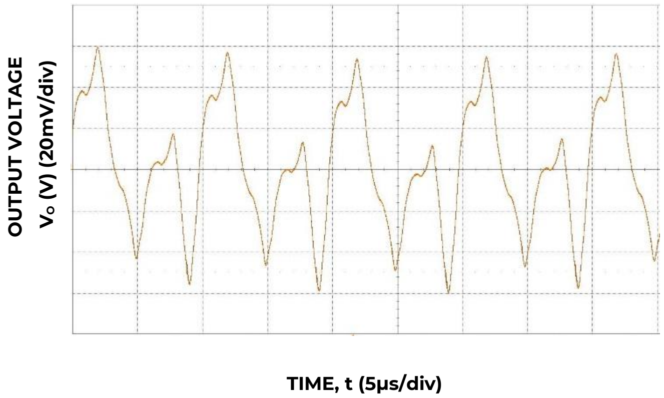


Figure 22. Typical Output Ripple at 48V Input, $I_{O,max}$ and C_O = 1x0.1μF, 6x1uF, 10x10uF (ceramics) and 220uF (electrolytic).

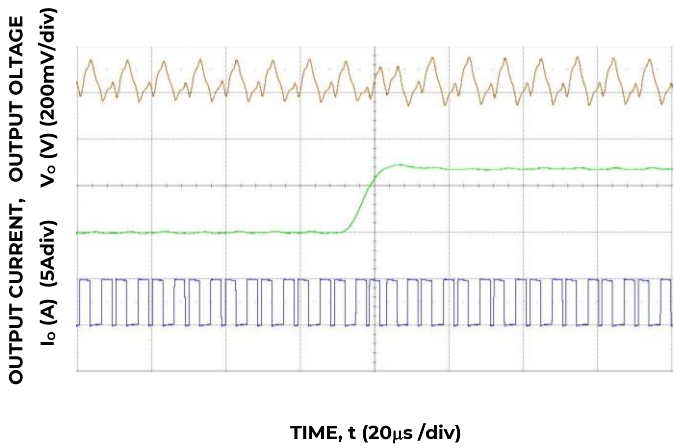


Figure 23. Transient Response to Dynamic Load Change from 50% to 100% at 48V_{IN}, C_O = 1x0.1μF, 6x1uF, 10x10uF (ceramics) and 220uF (electrolytic).

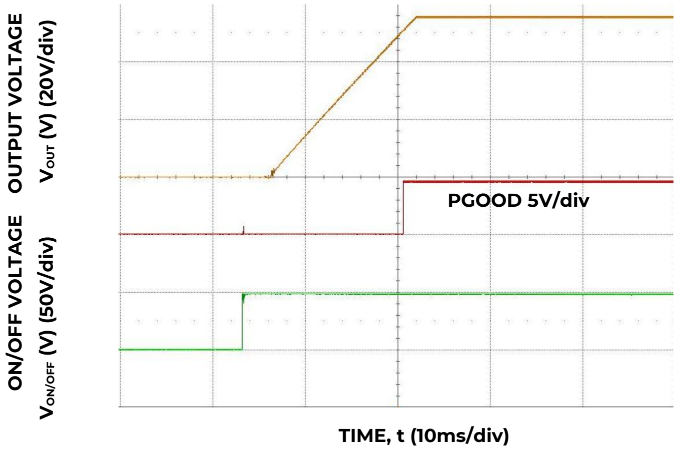


Figure 24. Typical Start-up Using On/Off Voltage (V_{IN} = 48V, $I_{O,max}$).

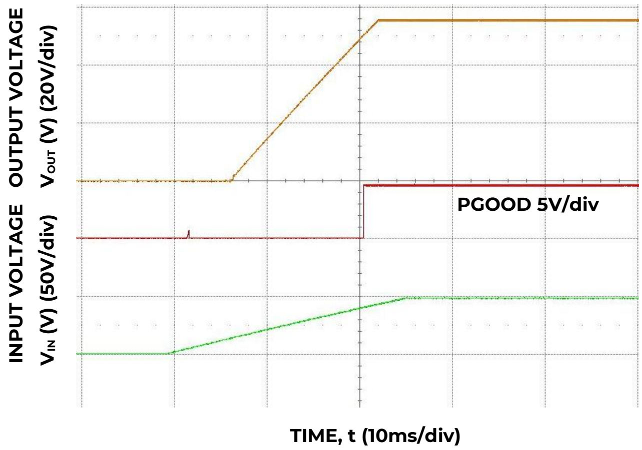
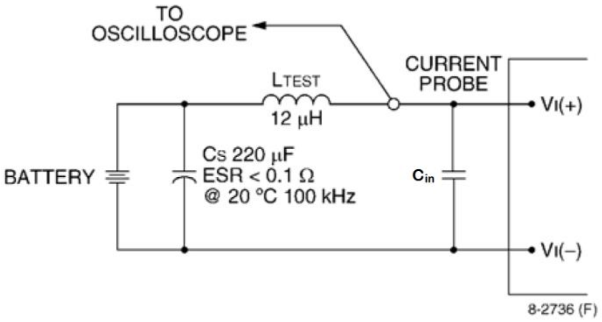


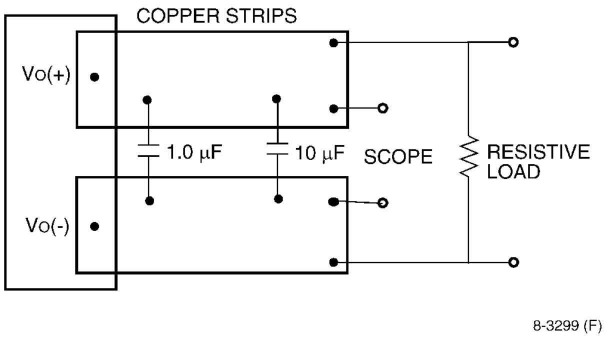
Figure 25. Typical Start-up Using Input Voltage (V_{IN} = 48V, $I_{O,max}$).

Test Configurations



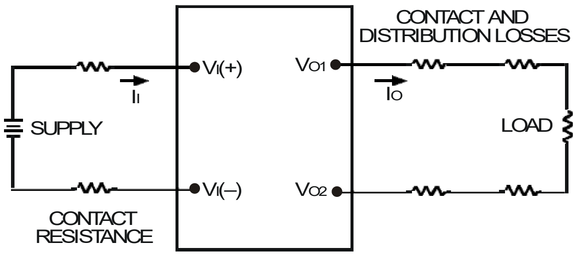
Note: Measure input reflected-ripple current with a simulated source inductance (LTEST) of 12 µH. Capacitor CS offsets possible battery impedance. Measure current as shown above.

Figure 26. Input Reflected Ripple Current Test Setup.



Note: Use a 1.0 µF ceramic capacitor and a 10 µF capacitor. Scope measurement should be made using a BNC socket. Position the load between 51 mm and 76 mm (2 in. and 3 in.) from the module.

Figure 27. Output Ripple and Noise Test Setup.



Note: All measurements are taken at the module terminals. When socketing, place Kelvin connections at module terminals to avoid measurement errors due to socket contact resistance.

$$\eta = \left(\frac{[V_O(+) - V_O(-)]I_O}{[V_I(+) - V_I(-)]I_I}\right) \times 100\ \%$$

Figure 28. Output Voltage and Efficiency Test Setup.

Design Considerations

Input Filtering

The 5-59V ProLynx2 module should be connected to a low ac-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Figure 29 and 30 shows the input ripple voltage for various output voltages at maximum load current with the stated ceramic capacitors.

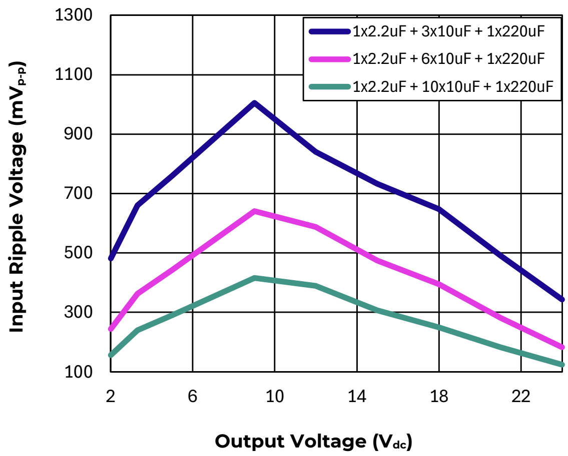


Figure 29. Input ripple voltage for various output voltages with incremental ceramic capacitors at the input (maximum load). Input voltage is 28V.

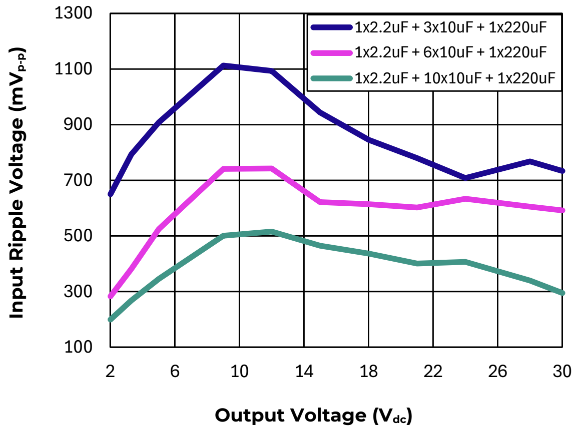


Figure 30. Input ripple voltage for various output voltages with incremental ceramic capacitors at the input (maximum load). Input voltage is 48V.

Output Filtering

The 5-59V ProLynx2 modules are designed for low output ripple voltage and will meet the maximum output ripple specification with the stated ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for several reasons. First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. Figures 31 and 32 provides output ripple information for different external capacitance values at various Vo and for full load currents. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table.

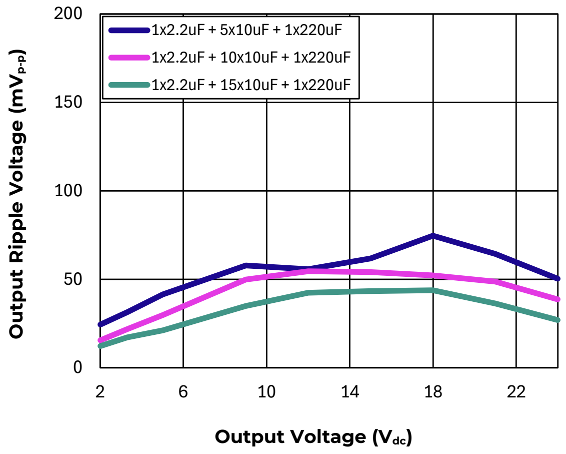


Figure 31. Output ripple with stated external ceramic capacitors at the output (max. load). Input voltage is 28V. Scope BW at 20MHz.

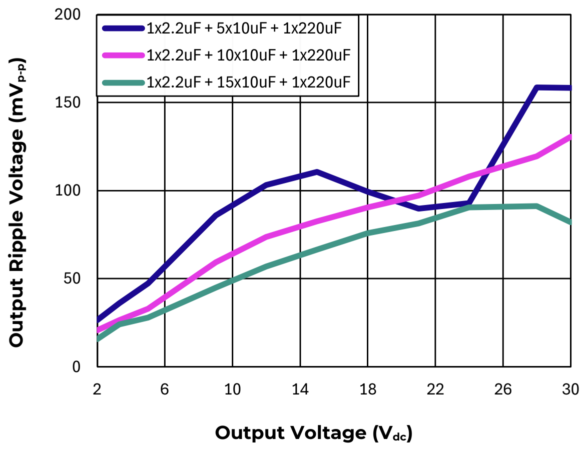


Figure 32. Output ripple with external ceramic capacitors at the output (max. load). Input voltage is 48V. Scope BW at 20MHz.

Safety Considerations

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL ANSI/UL* 62368-1 and CAN/CSA+ C22.2 No. 62368-1 Recognized, DIN VDE 0868-1/ A11:2017 (EN62368-1:2014/A11:2017) all pending.

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV) or ES1, the input must meet SELV/ES1 requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.

The input to these units is to be provided with a Fast-Acting ceramic fuse in the positive input lead. For input voltages less than $20V_{dc}$ use a fuse with maximum rating of 25A and for input voltages greater than $20V_{dc}$ use a fuse with maximum rating of 12A.

Feature Descriptions

Remote On/Off

The 5-59V ProLynx2 modules feature an EN pin for remote enable operation. In the Positive Logic EN feature, (device code suffix "4" – see Ordering Information), the module turns ON during a logic High on the EN pin and turns OFF during a logic Low.

If using an external voltage source for EN, the maximum voltage on the EN pin must always be less than V_{IN} in any operating/energized situation. Also, do not connect EN directly to V_{IN}.

For ease of use it is recommended to connect the EN pin to the midpoint of a resistor divider between V_{IN} and AGND as shown below in Figure 33. Using a 51kΩ for R_{TOP} and 19.6kΩ for R_{BOT} will allow the module to automatically turn on once V_{IN} is detected for all input/output voltage conditions.

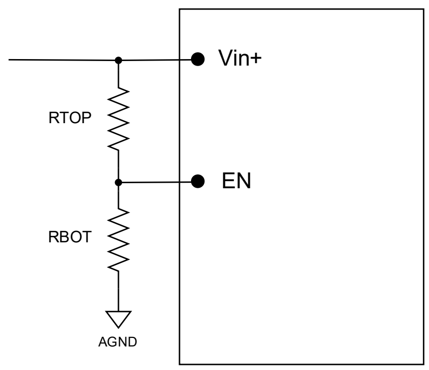


Figure 33. On/Off Implementation Using Resistor Divider.

Input Undervoltage Lockout

At input voltages below the input undervoltage lockout limit, the module operation is disabled. The module will begin to operate at an input voltage above the under-voltage lockout turn-on threshold.

Output Voltage Programming

The output voltage of the 5-59V ProLynx2 module can be programmed to any output voltage from $2V_{dc}$ to $30V_{dc}$ by connecting a resistor, R_{trim}, between the VS+ and VS- pins as shown in figure 34.

Certain restrictions apply on the output voltage set point depending on the input voltage. Figure 35 shows the maximum output voltage capability for a given input voltage. Figure 36 shows the maximum output current capability. For constant operating the value of output power (V_{OUT} x I_{OUT}) should not exceed 150W.

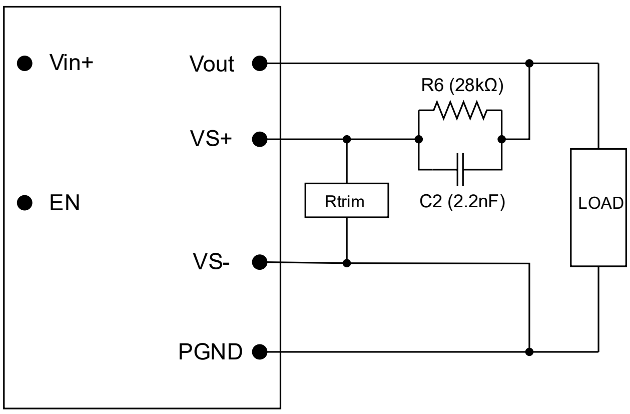


Figure 34. Circuit configuration for programming output voltage using an external resistor.

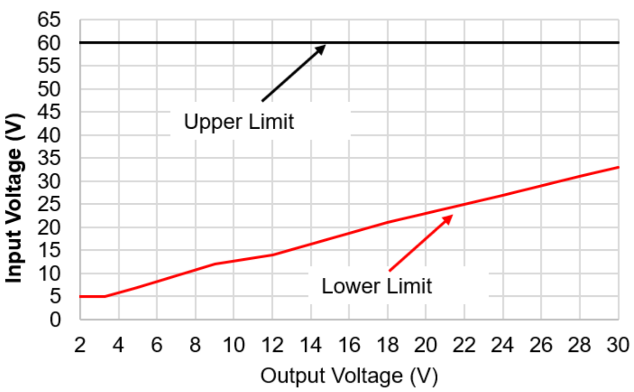


Figure 35. Graph showing maximum output voltage capability at different input voltages.

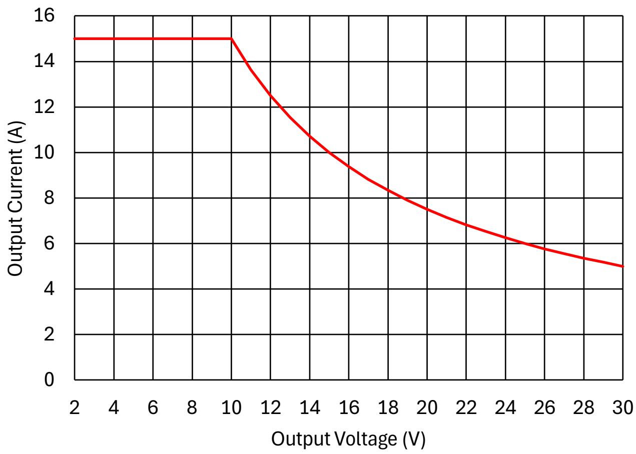


Figure 36. Graph showing maximum output current capability at different output voltages

Table 1 provides R_{trim} values required for some common output voltages.

Table 1

$V_{O, set}$ (V)	R_{trim} (KΩ)
2	12
2.5	8.84
3	7
3.3	6.22
5	3.82
6	3.11
9	2
12	1.47
15	1.17
18	0.97
21	0.82
24	0.72
28	0.61
30	0.57

To calculate the value of the trim resistor, R_{trim}, for a desired output voltage use the following equation:

$$Rtrim = \frac{16.8\ x\ 10^3}{Vout - 0.6}\ ohms$$

By using a ±0.1% tolerance trim resistor with a TC of ±100ppm, a set point tolerance of +/-1% (maximum) can be achieved as specified in the electrical specification. If desired R_{trim} value cannot be achieved with a single resistor, it is acceptable to use two resistors in series.

Remote Sense

The ProLynx2 power modules have a differential Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the VS+ and VS- pins (voltage across the R_{trim} resistor) to 0.6V. Connect VS+ to the parallel combination of R6 & C2, then route the trace differentially with VS- to desired output sense location (see Figure 36).

Output Overvoltage Protection

The ProLynx2 module features output overvoltage protection (OVP) which will trigger the module to latch-off and stop switching. After a latch-off the module requires either cycling input power or voltage on the EN pin to turn the module back on.

OVP is detected across the VS+ and VS- pins. When the differential voltage across these pins increases from its steady state value of 0.6V to 0.672 (typ. 12% increase) the module will trigger OVP protection and latch-off.

Output Overcurrent Protection

To provide protection in a fault output overload condition, the unit is equipped with internal current limiting circuitry and can endure current limiting continuously. At the point of current-limit inception, the unit enters hiccup mode. The unit operates normally once the output current is brought back into its specified range. For constant operation the value of output power (V_{OUT} x I_{OUT}) should not exceed 150W.

The current limit is set by connecting a resistor between the ILIM pin and AGND. The following tables show the appropriate current limiting resistor values for a given operating range and application circuit. Use a ±0.1% tolerance resistor with a TC of ±100ppm.

Table 2: Application Circuits #1, #2, and #3

V_{IN} (V)	V_{OUT} (V)	ILIM (KΩ)
5 – 14	2 – 12	29.4
14.1 – 59	2 – 14	22.6
18 – 59	14.1 – 23.9	16.9
28 – 59	24 – 27.9	15.4
33 – 59	28 – 30	13.7

Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation.

Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Figure 38. The preferred airflow direction for the module is in Figure 39. The derating data applies to airflow in either direction of the module's short axis.

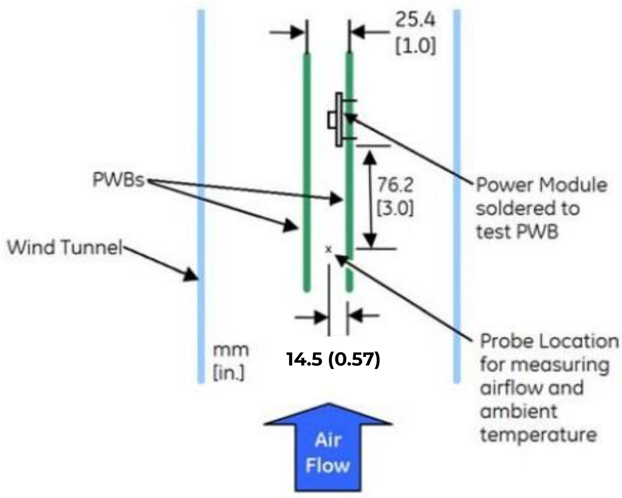


Figure 37. Thermal Test Setup

The thermal reference points, Tref used in the specifications are also shown in Figure 39. For reliable operation the temperatures at these points should not exceed 118°C. The output power of the module should not exceed the rated power of the module ($V_{O, set}$ x $I_{O, max}$).

Please refer to the Application Note "Thermal Characterization Process for Open-Frame Board-Mounted Power Modules" for a detailed discussion of thermal aspects including maximum device temperatures.

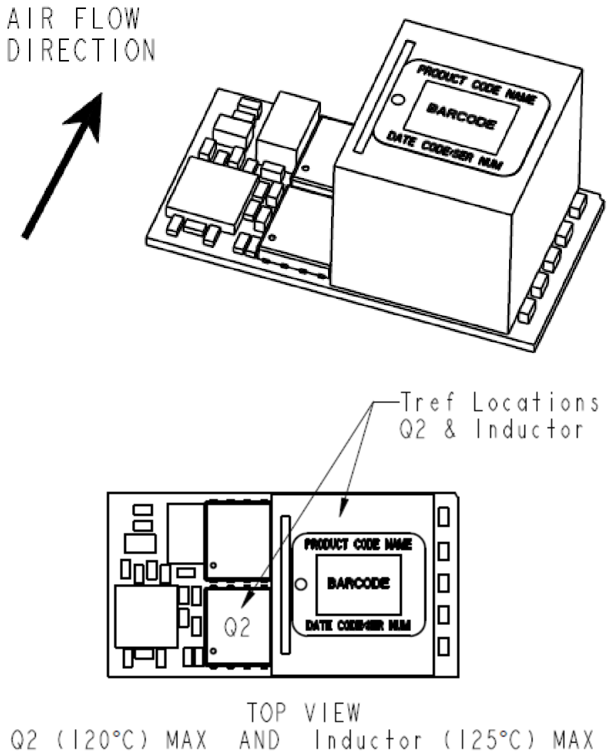


Figure 38. Preferred airflow direction and location of hot spot of the module (Tref)

Shock and Vibration

The ruggedized (-D version) of the modules are designed to withstand elevated levels of shock and vibration to be able to operate in harsh environments. The ruggedized modules have been successfully tested to the following conditions:

Non-operating random vibration:

Random vibration tests conducted at 25°C, 10 to 2000Hz, for 30 minutes each level, starting from 30Grms (Z axis) and up to 50Grms (Z axis). The units were then subjected to two more tests of 50Grms at 30 minutes each for a total of 90 minutes.

Operating shock to 40G per Mil Std. 810G, Method 516.4 Procedure I:

The modules were tested in opposing directions along each of three orthogonal axes, with waveform and amplitude of the shock impulse characteristics as follows:

All shocks were half sine pulses, 11 milliseconds (ms) in duration in all 3 axes.

Units were tested to the Functional Shock Test of MIL-STD-810, Method 516.4, Procedure I - Figure 516.4-4. A shock magnitude of 40G was utilized. The operational units were subjected to three shocks in each direction along three axes for a total of eighteen shocks.

Operating vibration per Mil Std 810G, Method 514.5 Procedure I:

The ruggedized (-D version) modules are designed and tested to vibration levels as outlined in MIL-STD-810G, Method 514.5, and Procedure 1, using the Power Spectral Density (PSD) profiles as shown in Table 1 and Table 2 for all axes. Full compliance with performance specifications was required during the performance test. No damage was allowed to the module and full compliance to performance specifications was required when the endurance environment was removed. The module was tested per MIL-STD-810, Method 514.5, Procedure I, for functional (performance) and endurance random vibration using the performance and endurance levels shown in Table 5 and Table 6 for all axes. The performance test has been split, with one half accomplished before the endurance test and one half after the endurance test (in each axis). The duration of the performance test was at least 16 minutes total per axis and at least 120 minutes total per axis for the endurance test. The endurance test period was 2 hours minimum per axis.

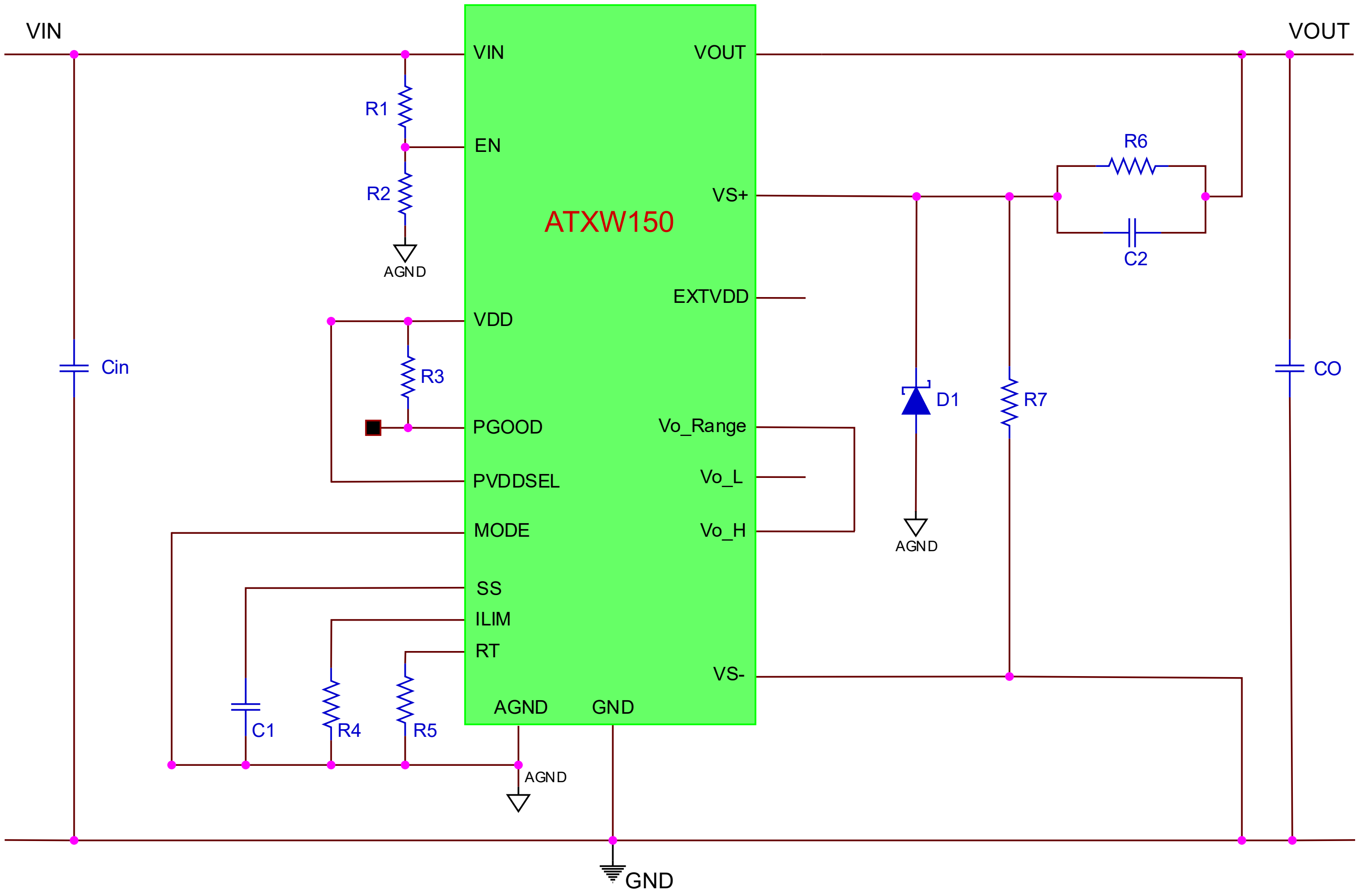
Frequency (Hz)	PSD Level (G2/Hz)	Frequency (Hz)	PSD Level (G2/Hz)	Frequency (Hz)	PSD Level (G2/Hz)
10	1.14E-03	170	2.54E-03	690	1.03E-03
30	5.96E-03	230	3.70E-03	800	7.29E-03
40	9.53E-04	290	7.99E-04	890	1.00E-03
50	2.08E-03	340	1.12E-02	1070	2.67E-03
90	2.08E-03	370	1.12E-02	1240	1.08E-03
110	7.05E-04	430	8.84E-04	1550	2.54E-03
130	5.00E-03	490	1.54E-03	1780	2.88E-03
140	8.20E-04	560	5.62E-04	2000	5.62E-04

Frequency (Hz)	PSD Level (G2/Hz)	Frequency (Hz)	PSD Level (G2/Hz)	Frequency (Hz)	PSD Level (G2/Hz)
10	0.00803	170	0.01795	690	0.00727
30	0.04216	230	0.02616	800	0.05155
40	0.00674	290	0.00565	890	0.00709
50	0.01468	340	0.07901	1070	0.01887
90	0.01468	370	0.07901	1240	0.00764
110	0.00498	430	0.00625	1550	0.01795
130	0.03536	490	0.01086	1780	0.02035
140	0.0058	560	0.00398	2000	0.00398

Application Circuit #1

V_{IN}: 16 – 59V

V_{OUT}: 14.1 – 30V (step down conversion only; based on value of V_{IN} – See Figure 35).



Cin – Input capacitor bank, 1x220µF + 5x10µF + 1x0.1µF (100V rated)

CO – Output capacitor bank, 1x220µF + 10x10µF + 1x0.1µF (50V rated)

C1 – 33nF ceramic

C2 – 2.2nF ceramic

R1 – R_{TOP} Enable Pin Resistor Divider (default 51kΩ)

R2 – R_{BOTTOM} Enable Pin Resistor Divider (default 19.6kΩ)

R3 – 20kΩ

R4 – Current Limit Resistor (See Table 2)

R5 – 255kΩ

R6 – 28kΩ

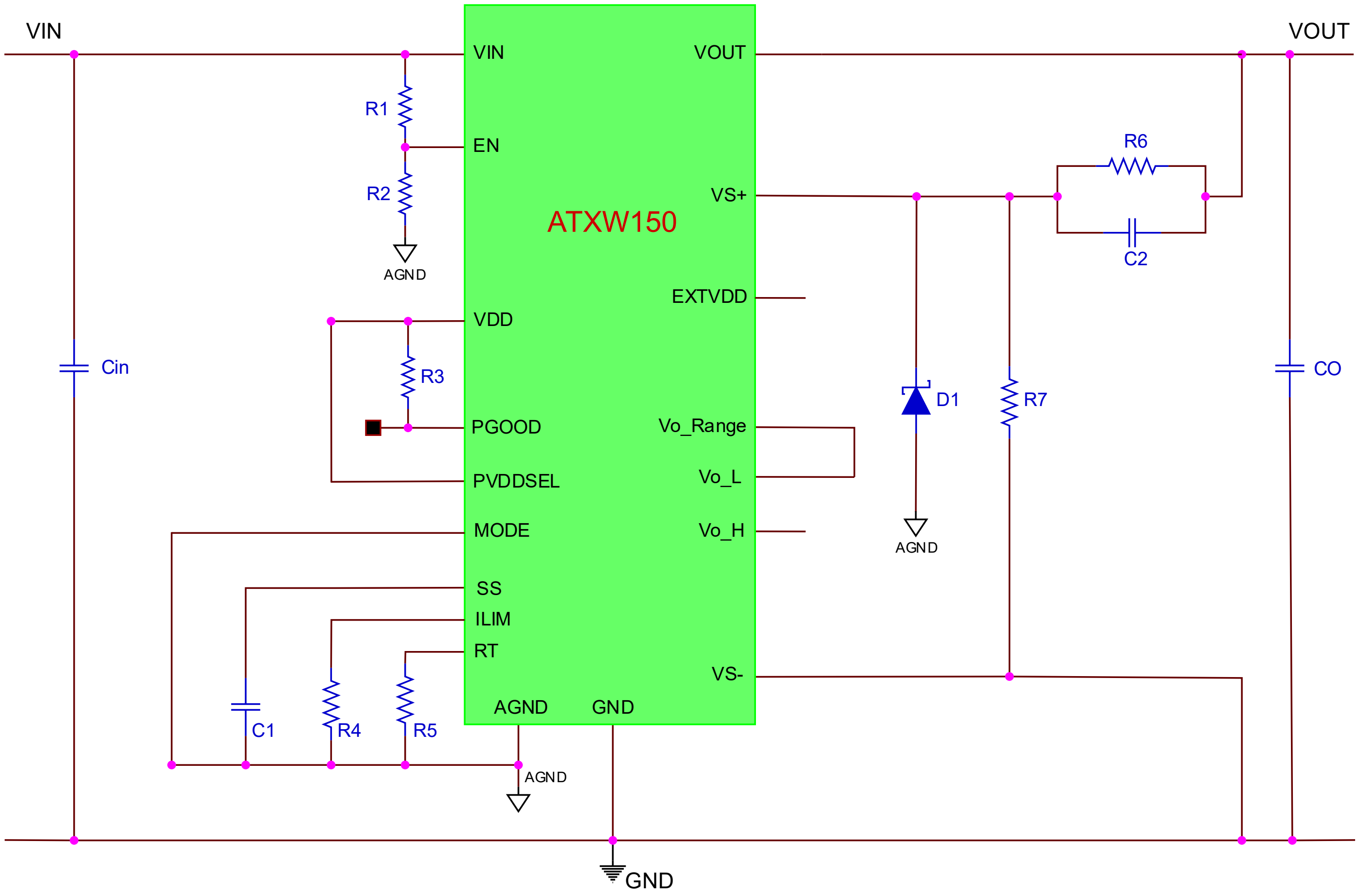
R7 – Rtrim (V_{OUT} Setting Resistor – See Table 1)

D1 – Schottky Diode, RB751S40T5G or equivalent. Must have reverse leakage current of <=2uA for blocking voltage of 0.6V at corresponding ambient temp.

Application Circuit #2

V_{IN}: 14.1 – 59V

V_{OUT}: 2 – 14V (step down conversion only; based on value of V_{IN} – See Figure 35).



Cin – Input capacitor bank, 1x220µF + 5x10µF + 1x0.1µF (100V rated)

CO – Output capacitor bank, 1x220µF + 10x10µF + 1x0.1µF (50V rated)

C1 – 33nF ceramic

C2 – 2.2nF ceramic

R1 – R_{TOP} Enable Pin Resistor Divider (default 51kΩ)

R2 – R_{BOTTOM} Enable Pin Resistor Divider (default 19.6kΩ)

R3 – 20kΩ

R4 – Current Limit Resistor (See Table 2)

R5 – 102kΩ

R6 – 28kΩ

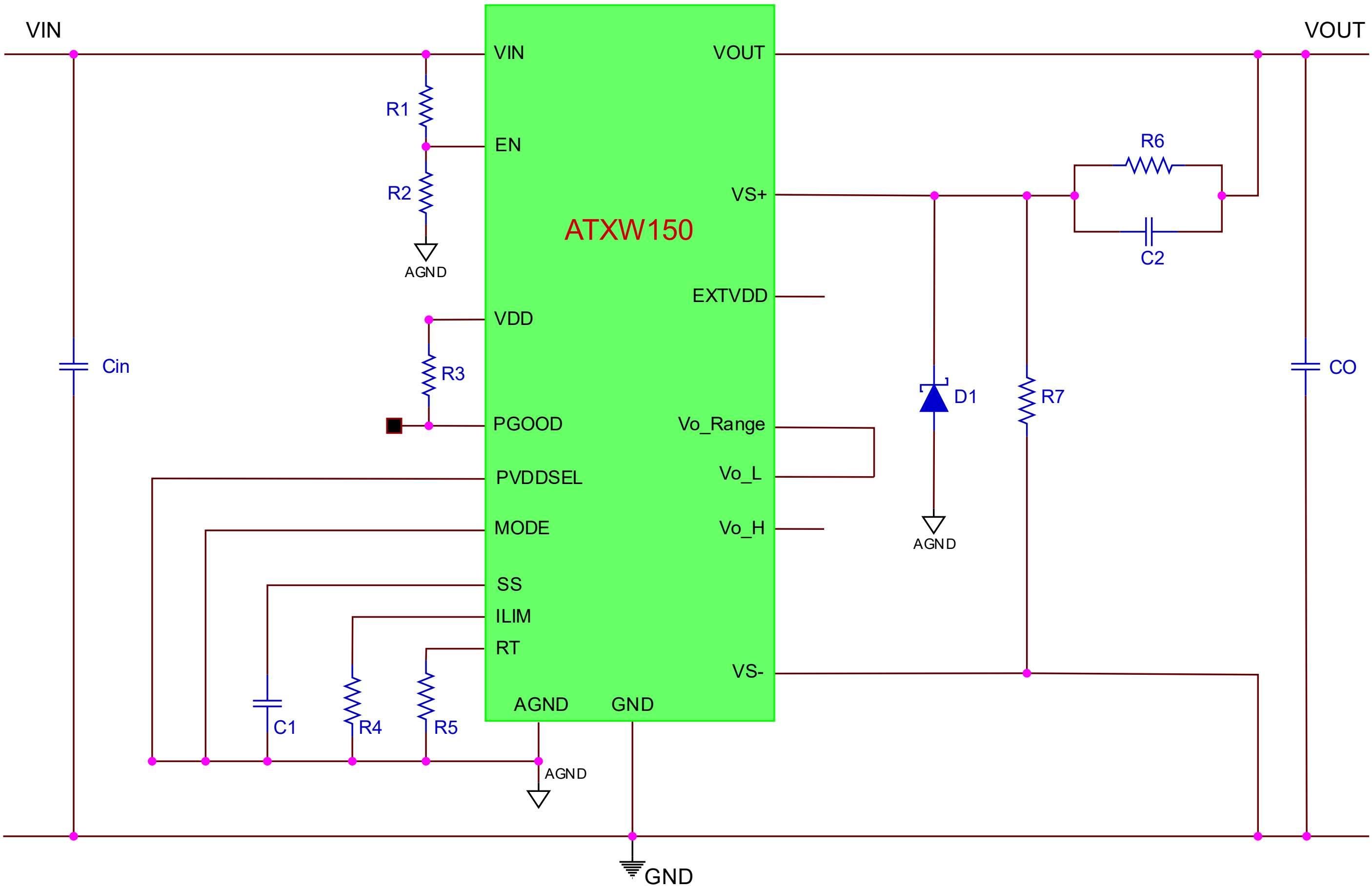
R7 – Rtrim (V_{OUT} Setting Resistor – See Table 1)

D1 – Schottky Diode, RB751S40T5G or equivalent. Must have reverse leakage current of <=2uA for blocking voltage of 0.6V at corresponding ambient temp.

Application Circuit #3

V_{IN}: 5 – 14V

V_{OUT}: 2 – 12V (step down conversion only; based on value of V_{IN} – See Figure 35 in this Datasheet).



Cin – Input capacitor bank, 1x220µF + 5x10µF + 1x0.1µF (100V rated)

CO – Output capacitor bank, 1x220µF + 10x10µF + 1x0.1µF (50V rated)

C1 – 33nF ceramic

C2 – 2.2nF ceramic

R1 – R_{TOP} Enable Pin Resistor Divider (default 51kΩ)

R2 – R_{BOTTOM} Enable Pin Resistor Divider (default 19.6kΩ)

R3 – 20kΩ

R4 – Current Limit Resistor (See Table 2)

R5 – 102kΩ

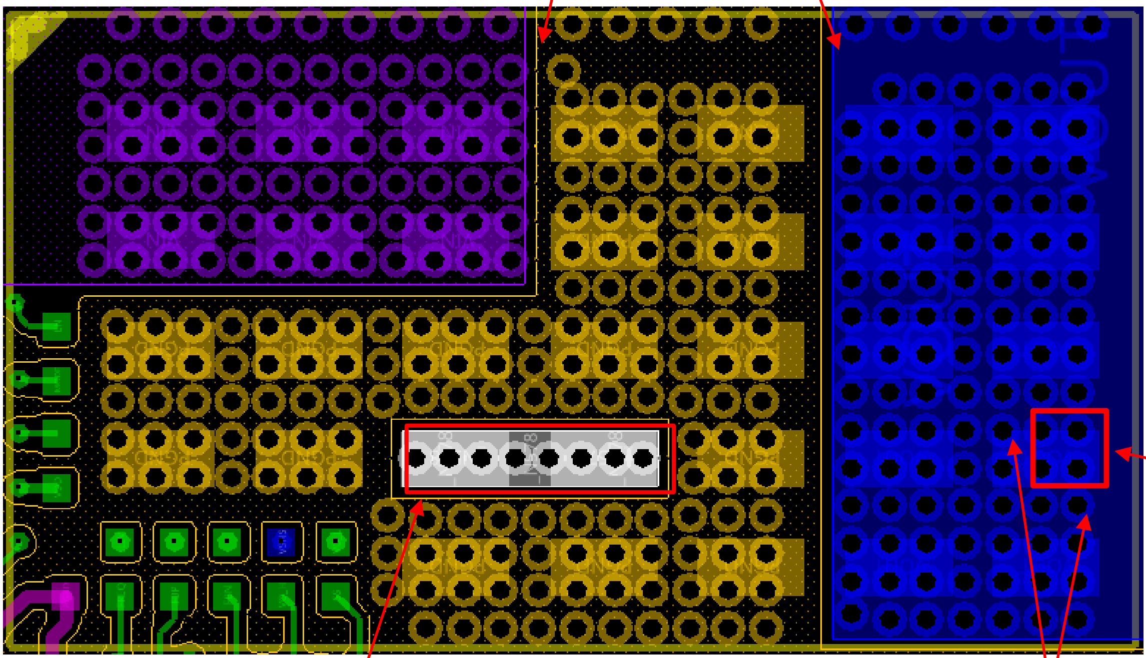
R6 – 28kΩ

R7 – Rtrim (V_{OUT} Setting Resistor – See Table 1)

D1 – Schottky Diode, RB751S40T5G or equivalent. Must have reverse leakage current of <=2uA for blocking voltage of 0.6V at corresponding ambient temp.

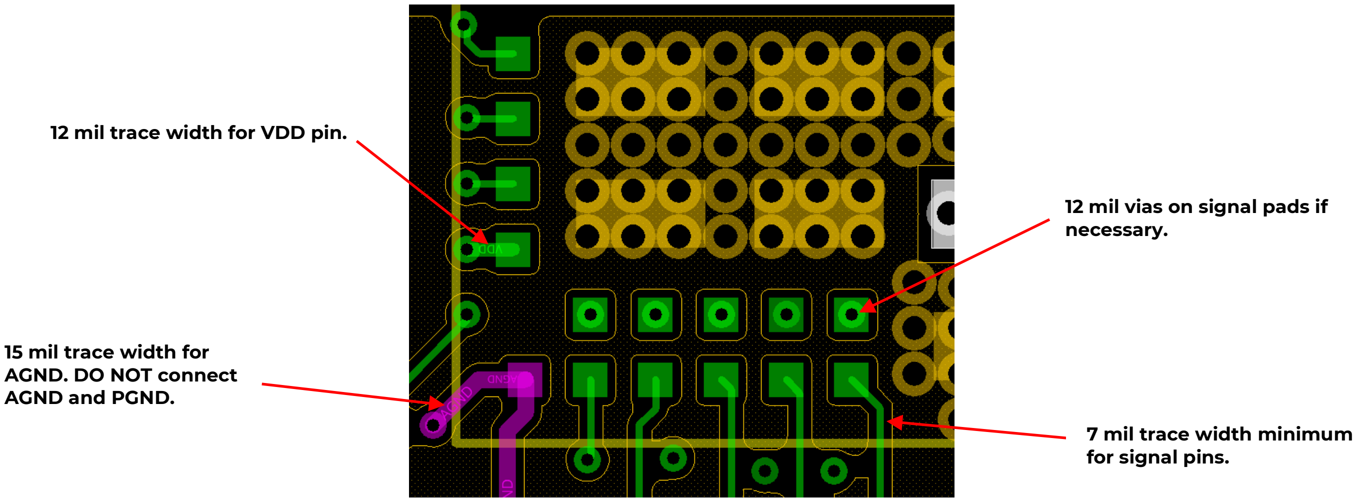
Layout Guidelines

For thermal and current carrying considerations, it is recommended to use at least four 22mil filled vias for each power pin. If space allows add extras vias around the pins in the respective plane. 12 mil filled vias recommended for signal pins as necessary. Use 3oz copper for inner layers and ¼oz copper for outer layers. Provide at least 24 mil spacing between power planes.

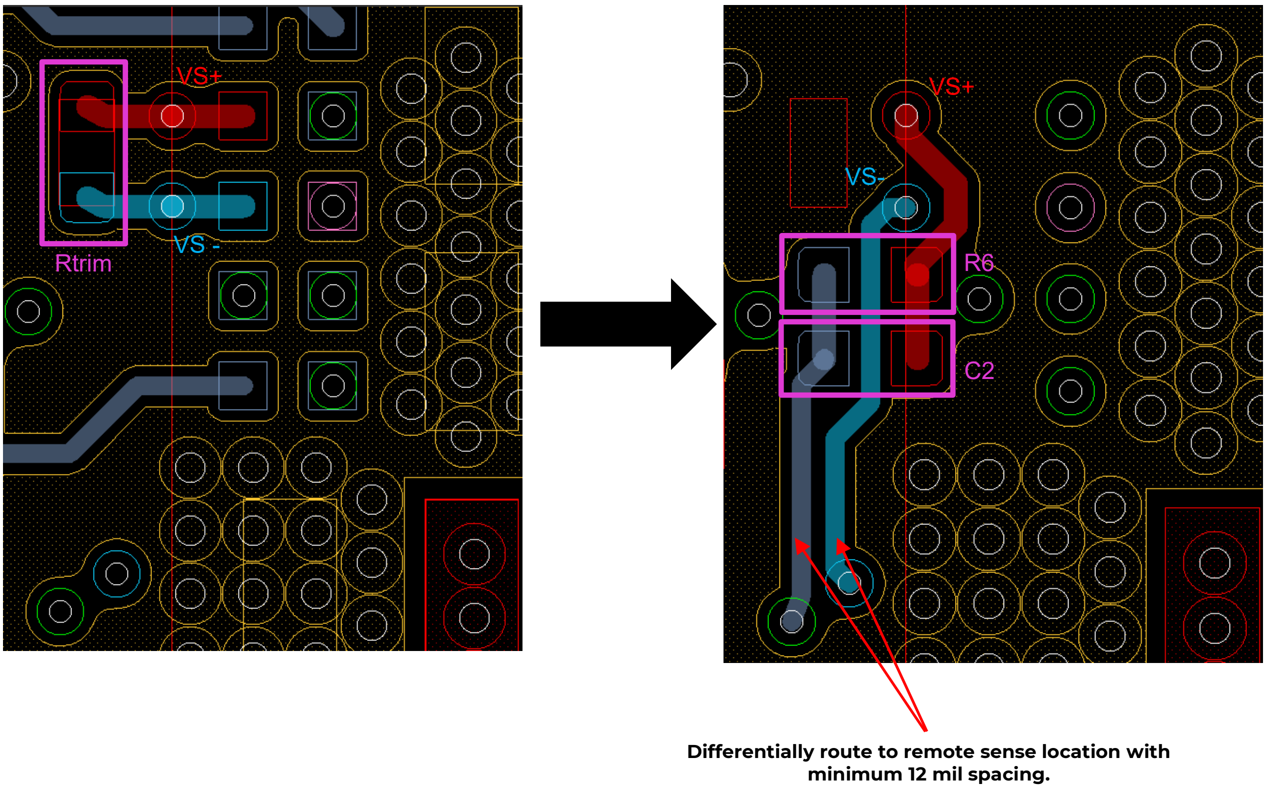


(TOP VIEW)

Layout Guidelines (continued)



Ensure that all the necessary connections for the VS+ node are made. VS+ needs to be connected to the cathode of the Schottky diode (D1), the Rtrim resistor, and the parallel combination of R6 & C2. Furthermore, after connecting VS+ to the R6 & C2 route the other end of this parallel combination with VS- to the desired sense location with at least 12 mil spacing. An example can be seen below:



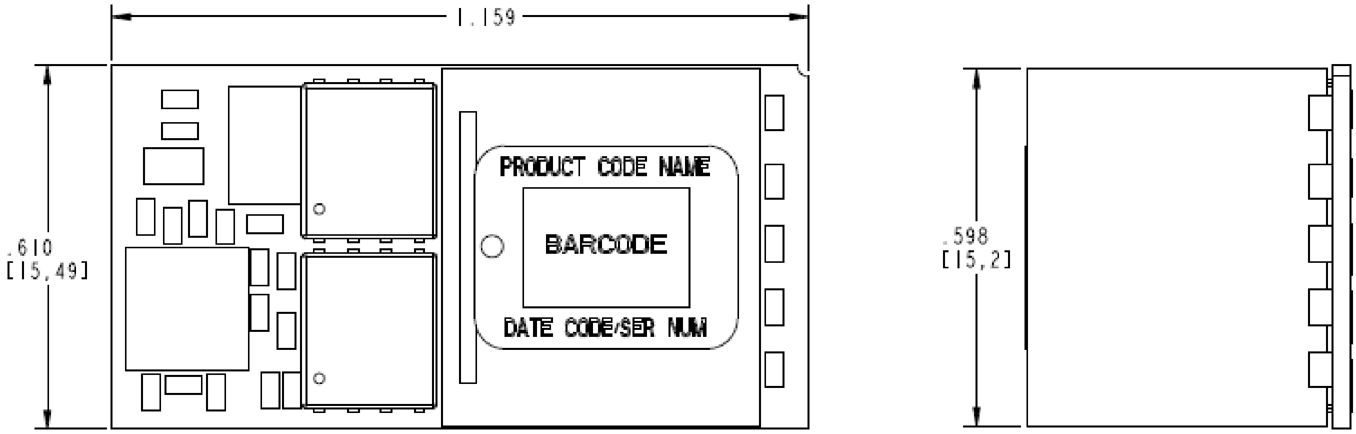
Mechanical Outline

Dimensions are in millimeters and (inches).

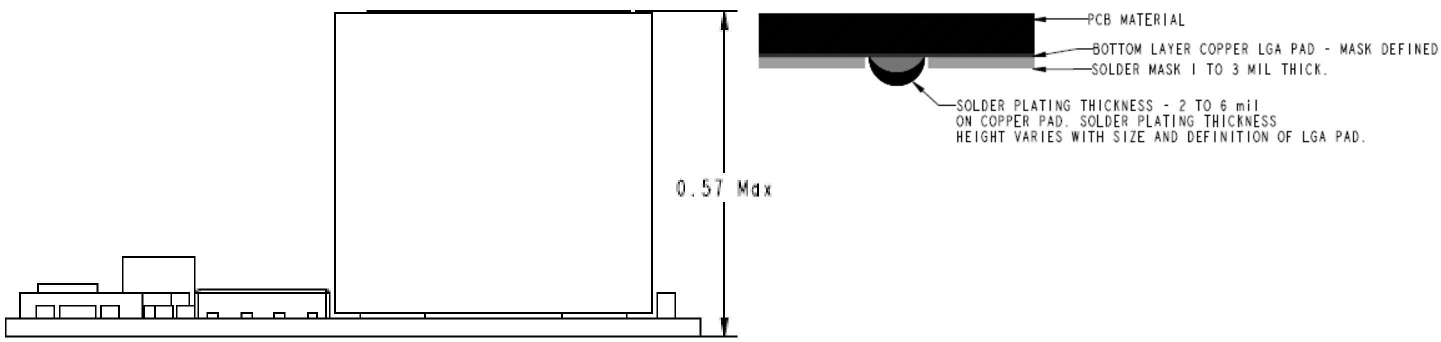
Tolerances: x.x mm ± 0.5 mm (x.xx in. ± 0.02 in.) [unless otherwise indicated]

x.xx mm ± 0.25 mm (x.xxx in ± 0.010 in).

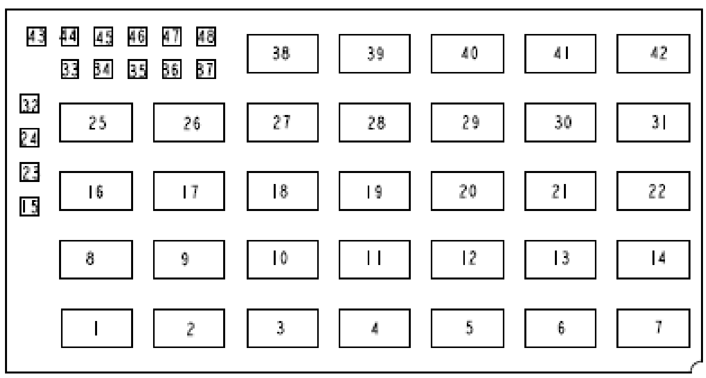
TOP VIEW



FRONT VIEW



BOTTOM VIEW

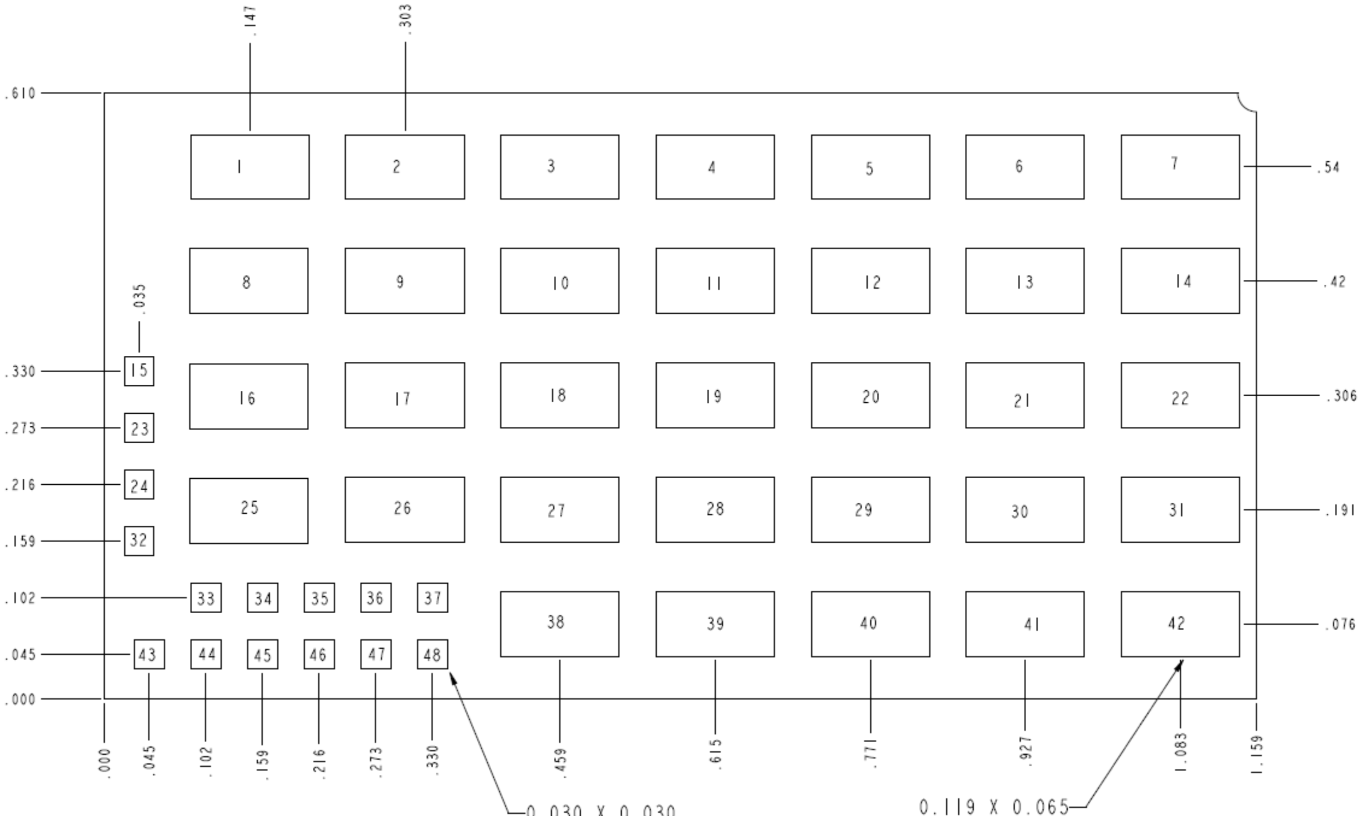


Recommended Pad Layout (Top View)

Dimensions are in millimeters and (inches).

Tolerances: x.x mm ± 0.5 mm (x.xx in. ± 0.02 in) [unless otherwise indicated]

x.xx mm ± 0.25 mm (x.xxx in ± 0.010 in).



PIN	FUNCTION	PIN	FUNCTION
1	VIN	25	PGND
2	VIN	26	PGND
3	VIN	27	EP
4	PGND	28	EP
5	PGND	29	PGND
6	VOUT	30	VOUT
7	VOUT	31	VOUT
8	VIN	32	VDD
9	VIN	33	ILIM
10	VIN	34	EXTVDD
11	PGND	35	PGOOD
12	PGND	36	Vo_Range
13	VOUT	37	Vo_L
14	VOUT	38	PGND
15	EN	39	PGND
16	PGND	40	PGND
17	PGND	41	VOUT
18	PGND	42	VOUT
19	PGND	43	AGND
20	PGND	44	RT
21	VOUT	45	VS+
22	VOUT	46	VS-
23	MODE	47	Vo_H
24	PVDDSEL	48	SS

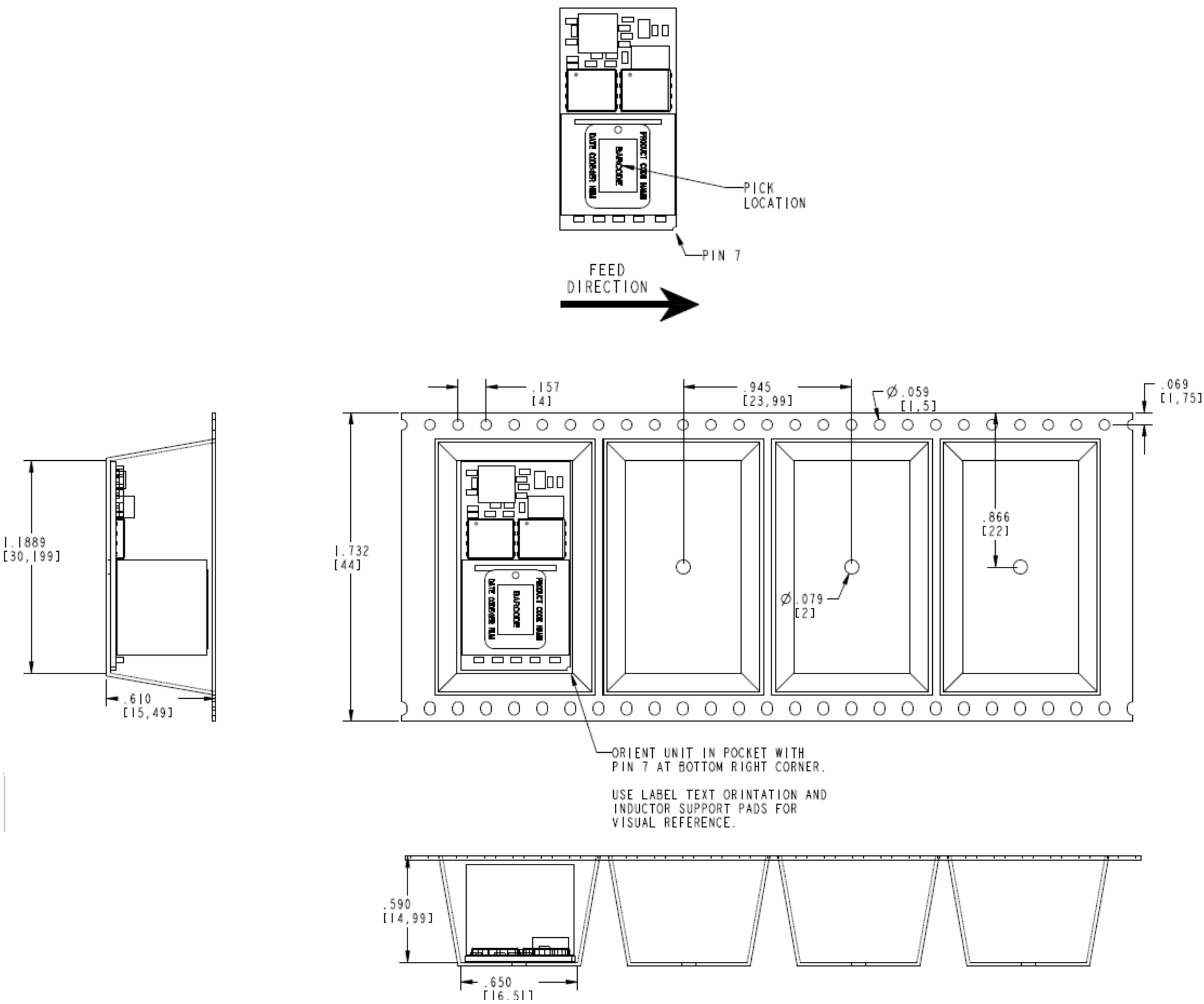
Module Pin Description

Function	Comments
V_{IN}	Input Voltage, positive polarity.
PGND	Power Ground. **DO NOT** connect to AGND.
V_{OUT}	Output Voltage, positive polarity.
EN	On/Off, Enable Pin. Since the module is positive polarity, Pin Voltage must be > On Threshold to start switching conversion. **CANNOT** be left floating.
MODE	Connect the MODE pin to AGND to select Continuous Conduction Mode (CCM). **CANNOT** be left floating.
PVDDSEL	Used for internal bias circuitry. Connect to AGND if V_{IN} ≤ 14V. Connect to VDD if V_{IN} > 14. **CANNOT** be left floating.
EP	Exposed Pad. Connect EP to isolated copper for best thermal performance (see layout considerations). **DO NOT** connect to PGND or AGND.
VDD	Internal 4.5V Bias LDO output. **DO NOT** use for external circuits.
ILIM	Current Limit Threshold Programming Input. Resistor between ILIM and AGND sets the current limit threshold.
EXTVDD	Float.
PGOOD	Open Drain Power Good Output. PG is low when the VS+ voltage is <83% of setpoint. Connect a pull-up resistor from PG to a pull-up source to set the PG voltage.
Vo_Range	Output voltage range selection input. Connect to either Vo_L or Vo_H. **CANNOT** be left floating.
Vo_L	Lower Output Voltage Range Connection Terminal. Connect to Vo_Range if V_{OUT} ≤ 14V, otherwise leave floating.
AGND	Analog ground. **DO NOT** connect to PGND.
RT	Timing Resistor Input. Resistor between RT and AGND sets switching frequency to 200kHz. Use a 102kΩ resistor if V_{OUT} ≤ 14V. Use a 255kΩ resistor if V_{OUT} > 14V. **CANNOT** be left floating.
VS+	Feedback Sense Input.
VS-	Feedback Ground Input.
Vo_H	Higher Output Voltage Range Connection Terminal. Connect to Vo_Range if V_{OUT} > 14V, otherwise leave floating.
SS	Soft Start Control. A 33nF ceramic capacitor is required between SS and AGND for a stable output voltage rise. **CANNOT** be left floating.

Packaging Details

The 5-59V ProLynx2 modules are supplied in tape & reel as standard. Modules are shipped in quantities of 100 modules per reel.

All Dimensions are in millimeters and (in inches).



Reel Dimensions:

Outside Dimensions:	330.2 mm (13.00 inches)
Inside Dimensions:	177.8 mm (7.00 inches)
Tape Width:	44 mm

Surface Mount Information

Pick and Place

The 5-59V ProLynx2 modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300°C. The label also carries product information such as product code, serial number and the location of manufacture.

Nozzle Recommendations

The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 6 mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 12 mm.

Bottom Side / First Side Assembly

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Lead Free Soldering

The 5-59V ProLynx2 modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

Pb-free Reflow Profile

Power Systems will comply with J-STD-020 Rev. D (Moisture/Reflow Sensitivity Classification for No hermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended linear reflow profile using Sn/Ag/Cu solder is shown in Figure 41. Soldering outside of the recommended profile requires testing to verify results and performance. For questions regarding Land grid array (LGA) soldering, solder volume; please contact OmniOn Power™ for special manufacturing process instructions.

MSL Rating

The 5-59V ProLynx2 modules have a MSL rating of 3.

Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture/ Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of ≤30°C and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40° C, < 90% relative humidity.

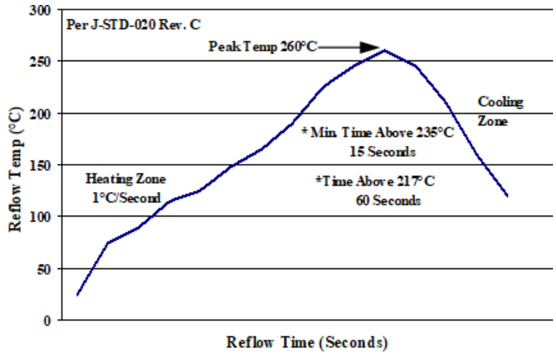


Figure 39. Recommended linear reflow profile using Sn/Ag/Cu solder.

Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to Board Mounted Power Modules: Soldering and Cleaning Application Note (AN04-001).

Ordering Information

Please contact your OmniOn Power™ Sales Representative for pricing, availability and future variants.

Table 3. Device Codes

Device Code	Input Voltage Range	Output Voltage	Output Current	On/Off Logic	Connector Type	Ordering Code
ATXW150WX43-SRDZ	5 – 59V_{dc}	2 – 30V_{dc}	15A – 5A	Positive	SMT	1600486860A

Table 4. Coding Scheme

TLynx family	Sequencing feature	Input voltage range	Output Power	Output voltage	On/Off logic	Remote Sense	Options		RoHS Compliance
AT	X	W	150	X	4	3	-SR	-D	Z
	X = w/o Seq	W = 5-59V	150W	X = programmable output	4 = positive No entry = negative	Available	S = Surface Mount R = Tape & Reel	D = 105°C Operating ambient, 40G Operating shock as per MIL Std 810G	Z = RoHS

Manufacturer Part Number	Ordering Code	Description
EVAL ATXW150	1600486916A	Evaluation Board withATXW150 module

Change History (excludes grammar and clarifications)

Revision	Date	Description of the change
1.0	1/16/2026	Initial Release

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