I^2C and PMBus™ Serial Communications Protocol

For the CAR Family of Power Supplies

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1 Introduction

The I²C interface incorporated within the CAR family of power supplies includes facilities to monitor and control various operating parameters within the unit and transmit these on demand over an industry standard I²C Serial bus. The CAR family of products supports two independent protocols. One is a OmniOn Energy developed interface that is significantly simpler than that required by the PMBus specifications. The second is a PMBus compliant interface. Both versions are supported in firmware at the same time. Either the OmniOn Energy developed interface or PMBus compliant commands could get executed at will in any desired combination.

1.1 Supported Functions

- Block Write – Block Read Process Call (Section 5.5.8 SMBus v2.0)
- Group Command Protocol (Section 5.2.3 PMBus v1.1X2)
- Linear Mode supported for all command/data transfers (Section 7.2 PMB v1.1X2) (Direct Mode NOT supported)
- Information in the registers will not be stored as defaults unless the command STORE_DEFAULT_ALL is executed

The detailed specifications for these products will reference this document for information on the communications protocol supported by the individual products. The product's detailed specifications may also highlight those commands that are not supported by that product. However, note that it is not mandatory for the product detailed specification to summarize non – supported commands. The protocol automatically notifies the host controller if a non – supported command has been transmitted.

2 Design Features

The following information represents a summary of functions provided by the microcontroller.

2.1 General Functions:

- Analog/PWM Control – Output Voltage, Current Limit, Fan Speed, Constant Power Operation
- Analog Reporting – Input Voltage, Output Voltage Sensing (Anode of Oring Device), Current and Temperature Monitor, Efficiency Optimization (Adjustable peaking between 30 – 50% load)
- Digital Reporting – Line sense, INPUT_OK, DC_OK, TEMP_OK, FAULT, OC, OVSD
- Digital Control – ON/OFF
- Calculation of Input Power Consumption
- EEPROM – Internal to MCU (96 Bytes)
- Serial Number/Part Number read – back from EEPROM
- I²C Clock stretching
- I²C Bus Lock – Up detection. The device will abort any transaction and drop off the bus if it detects the bus being held low for more than 35ms.

2.2 Electrical Interface

- Address lines (A0, A1, A2)
  These external address lines allow up to eight (8) CAR modules to be addressed on a single I²C bus.
- Serial Clock (SCL)
  This line is clocked by the host that controls the I²C serial bus.
- Serial Data (SDA)
  This is a bi – directional data line.
- Pull – up Resistors
  SDA and SCL lines have internal 10KW pull – up resistors and no more than 47pF of filtering capacitors. It is the end – user responsibility to ensure that signal rise and fall times meet I²C specifications.

2.3 EEPROM

The microcontroller has 96 bytes of EEPROM memory available for the system host. There is another External EEPROM IC that is separately addressable across the bus; it provides another 128 bytes of memory for storing manufacturing data. This External EEPROM is write protected via a signal pin on the power supply connector and is not for customer's use. The minimum information to be included in this External EEPROM is: model number, revision, date code, serial number etc.

3 Bus Communications

The Power Supply is a 'slave' device across the bus. As such, the power supply cannot initiate communications or 'take over' the bus. It only responds to instructions and commands transmitted by the 'host' controller.

The Power Supply adheres to both the I²C and SMBus hardware specification requirements. The mController and the EEPROM have their own embedded drivers for bus communications that are not controlled by the power supply.

3.1 PMBus Compliance Requirements

- Interoperability with I²C (as stated in Appendix B of SMBus v2.0)
- AC Specifications (must comply as stated in Table 2 – of Section 5.2.6 of PMB v1.1X2)
- DC Specifications (must comply with High Power DC Specifications of Section 3.1.3 SMBus v2.0)
- Signals and Controls
- 7 bit addressing (DO NOT use reserved Addresses in Appendix B of SMBus v2.0)
- Device must also respond to Global Broadcast address of 00h

3.2 SMBusAlert#

The SMBusAlert# (Interrupt) signal informs the 'host' controller that either a State or Alarm change has occurred. Normally this signal is HI. The signal will change to its LO level if the power supply has changed states and the signal will be latched LO until the power supply receives a 'clear' instruction as outlined below. If the alarm state is still present after the 'clear' instruction has been received then the signal will revert back into its LO level again and will latch until a subsequent 'clear' signal is received from the host controller.

The signal will be triggered for any state change, including the following conditions;

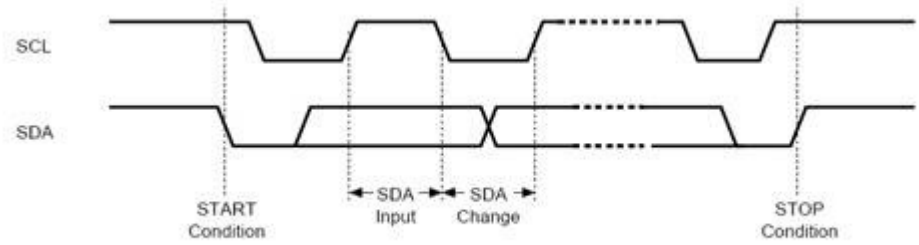
- V_{IN} under or over voltage, warning or fault
- V_{OUT} under or over voltage, warning or fault
- I_{OUT} over current, warning or fault
- Temperature under or over, warning or fault
- Active on Fan Failure
- Communication error
- PEC error
- Invalid command

The power supply will clear the SMBusAlert# signal (release the signal to its HI state) upon the following events:

- Receiving a CLEAR_FAULT command
- Turned OFF and then ON via the REMOTE ON/OFF signal pin
- Turned OFF and then ON by the COMMAND_OFF_I^2C instruction
- After a read to STATUS_BYTE (0x78) or STATUS_WORD (0x79) register

3.3 State Change of the data line (SDA)

The SDA line changes states when the clock is HI to signify when the START and STOP commands of the protocol are being sent. During data transmission, SDA can only change states when the clock is LO. When the clock is HI the devices interpret the SDA as a data bit of HI or LO. If the SDA would transition while the clock is HI, this would either indicate a RESTART or a STOP condition.



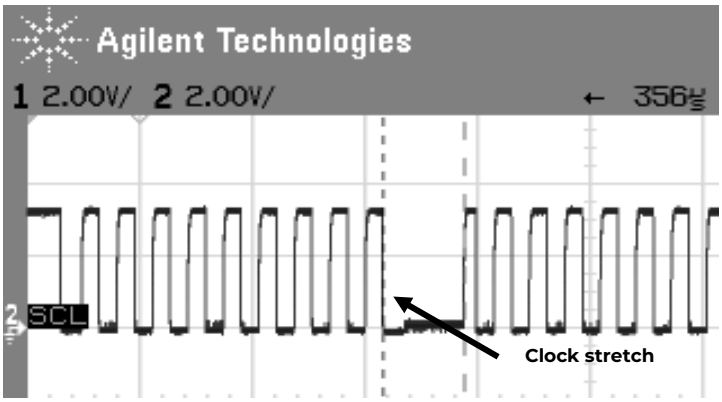
3.4 Clock speed

The CAR platform supports clock speeds up to 400 kHz. Bus capacitance is limited to 400pf including wire – length and internal device capacitance contributions. The minimum clock speed specified by SMBus is 10 kHz.

3.5 Clock (SCL) stretching

The mController inside the power supply initiates clock stretching, that is, stretch (keep the clock LO) until it is ready to receive further instructions from the host controller. The host controller needs to recognize this clock stretching, and refrain from issuing the next clock signal, until the clock line is released, or it needs to delay the next clock pulse beyond the clock stretch interval of the power supply.

A representative waveform below shows clock stretching. Probing of the SCL line shows who pulls down the clock. When the LO level is closer to GRD the power supply pulls down the clock. Clock stretching occurred after responding to the 'read' address of the mController. If the host supports clock stretching no further delay is required, the power supply will release the SCL signal when it is ready to send the data. The duration of clock stretch is program dependent and therefore it may differ among products. If the host does not support clock stretching, a delay would be required to delay the next clock pulse beyond the required delay interval.



3.6 Packet Error Checking (PEC)

Although the power supply will respond to commands without the trailing PEC based on the CRC – 8 format, the use of PEC is recommended. This trailing byte significantly improves the robustness of the protocol.

4 Communications improvements

The CAR family of power supplies will include command enhancements as new features are developed. When these features are form, fit, or function affecting then they will not be implemented until appropriate customer notifications have been sent out. However, if the new feature is an addition/enhancement that does not affect previous product revisions, then, no notifications are going to be sent out announcing these new features.

4.1 Output voltage control

The CAR family of power supplies has two independent means of output voltage control. The output voltage can be changed either by means of the Vprog hardware signal or by issuing a software command.

4.1.1 Early implementation

If Vprog control is implemented, it overrides any software issued commands as long as the Vprog level is below the voltage level documented in the individual product data sheets.

4.1.2 Improved implementation

Software issued commands override the Vprog hardware command. The intent is to allow the Vprog hardware command to set initial conditions prior to the establishment of communications, but, then allow a communications instruction to take over output voltage control. Once software takes over control, it keeps control until power is removed from the internal power supply controller. This condition clearly establishes who has control.

If power to the controller is interrupted, the controller will default to accepting the output voltage setting instructed by the hardware based Vprog pin until a subsequent software instruction tells the power supply to change the output voltage. This clearly establishes initial conditions for the power supply.

4.1.3 Documentation of the improvement

This improvement needs to be documented by a firmware revision upgrade.

5 Addressing

Device	Address	Address Bit Assignments (Most to Least Significant)							
MCU	0xBx	1	0	1	1	A2	A1	A0	R/W
All MCU (global)	0x00	0	0	0	0	0	0	0	W
EEPROM	0xAx	1	0	1	0	A2	A1	A0	R/W

A0, A1 & A2 are for setting 8 possible addresses by the user.

Normally there are up to four modules positioned across a 19" shelf. The modules are identified from left to right as:

MODULE 1	MODULE 2	MODULE 3	MODULE 4

Module addressing at the shelf level is configured by grounding the appropriate A1 and A0 signal pins of the power supply to the logic LO level:

	I²C address	
Rectifier	A1	A0
1	0	0
2	0	1
3	1	0
4	1	1

The A2 signal identifies either shelf 0 or shelf 1 in a multiple shelf configuration.

5.1 Global Broadcast

This is a powerful command because it can instruct all power supplies to respond simultaneously to the command. However, it does have an unfortunate limitation; Since all power supplies will pull down the ninth acknowledge [ACK] bit at the same time it is not known whether they all responded. To be certain that each power supply responded to the global instruction, a READ instruction should be executed to each power supply to verify that the command sent out by the Global Broadcast was properly executed.

The **Global Broadcast** instruction executes a simultaneous **write** instruction to all power supplies. A **read** instruction SHOULD NOT be accessed globally since multiple power supplies would respond back with a mixed set of data.

Instructions such as the setting of the output voltage should only be executed using the **Global Broadcast** in order to ensure proper current sharing and load delivery from the power supplies.

6 Standard Instructions

The standard **WRITE** instruction takes the form shown below. Up to two bytes of data may follow depending on required data content. PEC is not mandatory; it includes the address, command and data fields.

Note: Data fields are optional

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave address	Wr	A	Command Code	A	Low Data Byte	A	High Data Byte	A	PEC	A	P

☐ Clear area indicates Master to Slave communications
⬚ Shaded area indicates Slave to Master communications

I²C annotations;
S – Start, Wr – Write, Sr – re-Start, Rd – Read, A – Acknowledge, NA – not – acknowledged, P – Stop

The standard **READ** instruction has the following form:

1	7	1	1	8	1
S	Slave address	Wr	A	Command Code	A

1	7	1	1	8	1	8	1	8	1	1
Sr	Slave Address	Rd	A	LSB	A	MSB	A	PEC	No-ack	P

7 Block Instructions

When writing or reading more than two bytes of data at a time BLOCK instructions for WRITE and READ commands must be used instead of the Standard Instructions in Section 6 above to write any number of bytes greater than two.

Block Write format:

1	7	1	1	8	1	8	1	8	1		8	1	8	1	1
S	Slave address	Wr	A	Command Code	A	Byte Count = N	A	Data 1	A	...	Data 48	A	PEC	A	S

Block Read format:

1	7	1	1	8	1	1	7	1	1
S	Slave address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A

8	1	8	1		8	1	8	1	1
Byte Count = N	A	Data 1	A	...	Data 48	A	PEC	No – ack	S

WARNING: When using BLOCK WRITE on registers USER_DATA_00 and USER_DATA_01 (Registers 0xB0, 0xB1), each write should be done in 48 byte blocks; else the remaining bytes in memory will be corrupted. In other words, if a write of 8 bytes is done, the other 40 bytes will be corrupted.

8 I²C Protocol Register Set

The MCU has a set of registers described in the table below. Data is in Little Endian format (LSB followed by MSB). These registers allow a simpler way to communicate to the Power supply than that complying with the PMBus standard. Most of the I²C standard or Manufacturer specific commands are set at offset 0xB0 to 0xEF. To write/modify register contents the WRITE_PROTECT register (0x10) needs to be set to 0x00, else only the OPERATION and VOUT_COMMAND will be executed.

Access: RO = Read Only; R/W = Read/Write; Byte order is LSB first

The STATUS registers below comply with the requirements of the PMBus specification; a value of 1 indicates that a fault or warning event has occurred and a value of 0 indicates that the function is working normally. The exception is a register bit, such as STATUS_MFR_SPECIFIC bit 0, that provides operational information instead of a fault condition.

Source Parameter	Offset		Length	Access	Comments
CLEAR_FAULT	0x03		0	–	Clear fault/warning register and /SMBALERT signal
WRITE_PROTECT	0x10		1	R/W	Allow/Disable Write Access to registers
STATUS_WORD	0x79	0	2	RO	None of Below
		1			CML (communication fault) detected
		2			Temperature Fault/warning detected
		3			Input Under Voltage Fault detected
		4			Output Over Current Fault detected
		5			Output Over Voltage Fault detected
		6			PS is OFF
		7			Busy
		8			Unknown Error
		9			Other fault
		10			Fan Fault or Warning detected
		11			N/A
		12			Mfr Fault detected
		13			Input Fault/Warning detected
		14			Output Current Fault/Warning detected
		15			Output Voltage Fault/Warning detected
STATUS_VOUT	0x7A	0	1	RO	N/A
		1			N/A
		2			N/A
		3			N/A
		4			Vout Under Voltage Fault
		5			Vout Under Voltage Warning
		6			Vout Over Voltage Warning
		7			Vout Over Voltage Fault
STATUS_IOUT	0x7B	0	1	RO	N/A
		1			N/A
		2			N/A
		3			N/A
		4			N/A
		5			IOUT Over Current Warning
		6			N/A
		7			IOUT Over Current Fault
STATUS_INPUT	0x7C	0	1	RO	N/A
		1			N/A
		2			N/A
		3			N/A
		4			Vin Under Voltage Fault
		5			Vin Under Voltage Warning
		6			Vin Over Voltage Warning
		7			Vin Over Voltage Fault
STATUS_TEMPERATURE	0x7D	0	1	RO	N/A
		1			N/A
		2			N/A
		3			N/A
		4			Under Temperature Fault
		5			Under Temperature Warning
		6			Over Temperature Warning
		7			Over Temperature Fault

Source Parameter	Offset		Length	Access	Comments
STATUS_MFR_SPECIFIC	0X80	0	1	RO	0 = High Line/DC input; 1 = Low Line
		1			ACOK
		2			DCOK
		3			TEMP OK
		4			FAULT
		5			Interrupt
		6			OVSD
		7			Internal DC OK
STATUS_FAN_1_2	0x81	0	1	RO	N/A
		1			N/A
		2			Fan 2 Speed Overridden
		3			Fan 1 Speed Overridden
		4			N/A
		5			N/A
		6			Fan 2 Fault
		7			Fan 1 Fault
USER_DATA_00	0xB0		48	R/W	(Write/Read in 48 bytes block)
USER_DATA_01	0xB1		48	R/W	(Write/Read in 48 bytes block)
FRW_VERSION	0XD0		1	RO	High nibble: Major; Low nibble: Minor
Reserved	0xD1-0xD2				Reserved
ILIMIT_CTRL_I²C	0XD3		2	R/W	Current Limit Setting (1/100A)
VOUT_CTRL_I²C	0XD4		2	R/W	Output Voltage Setting (1/512V)
FAN_DUTY_CYCLE_I²C	0xD6		1	RO	Current Fan Duty Cycle (0 to 100%)
FAN_CONTROL_I²C	0xD7		1	R/W	Control Fan Duty Cycle (0 to 100%)
VPROG_EXT	0XD8		2	RO	External Voltage Programming
Reserved	0xD9-0xDF				Reserved
READ VOUT_I²C	0XE0		2	RO	Output Voltage (1/512V)
READ_IOUT_I²C	0XE1		2	RO	Output Current (1/100A)
READ_TS_I²C	0XE2		2	RO	Heat Sink Temperature (°C)
CMD_OFF_I²C	0XE3		2	R/W	1: OFF; 0: ON
OTF_LIMIT_I²C	0XE4		2	R/W	Over Temperature Fault Limit (°C)
OTF_RECOVERY_I²C	0XE5		2	R/W	Over Temperature Recovery (°C)
DCOKHI_I²C	0XE6		2	R/W	High Output Voltage fault limit (1/512V)
DCOKLO_I²C	0XE7		2	R/W	Low Output Voltage fault limit (1/512V)
Reserved	0xE8				Reserved
FAN1_SPEED_I²C	0xE9		2	RO	Fan #1 Speed (RPM)
FAN2_SPEED_I²C	0xEA		2	RO	Fan #2 Speed (RPM)
Reserved	0xEB				Reserved
Reserved	0xEC				Reserved
VIN_I²C	0xED		2	RO	Voltage Input (1/100V)
IIN_I²C	0xEE		2	RO	Input current (1/100A)
PIN_I²C	0xEF		2	RO	Input power (W)

Note: To have write access to a register the WRITE_PROTECT register needs to be set to 0x00.

9 Register Definitions

NOTE: All status registers except STATUS_MFR_SPECIFIC (Register 0x80) are reset to default or cleared under the following conditions:

- The Power supply receives a CLEAR_FAULT command
- Bias Power is removed from the power supply
- The power supply is turn OFF and then turn back ON

The STATUS_MFR_SPECIFIC register indicates the live status of the power supply at all times.

9.1 CLEAR_FAULT (Register 0x03)

Any warning or faults bits set in the status registers remain set; even if the fault or warning condition is removed or corrected, until one of the following occur:

- The Power supply receives a CLEAR_FAULT command
- Bias Power is removed from the power supply
- The power supply is turned OFF and then turned back ON.

The CLEAR_FAULT command will also deactivate the SMBAlert# signal.

If the fault or warning is still present after a CLEAR_FAULT command, the status register will again be updated and the SMBALERT# signal will be reactivated.

9.2 WRITE_PROTECT (Register 0x10)

The WRITE_PROTECT command is used to control writing to the Power Supply. The intent of this command is to provide protection against accidental changes or against a corrupted command due to noise on the communication lines. All supported commands may have their parameters read regardless of the WRITE_PROTECT settings.

This command has one data byte:

- 0x80 : Disable all writes except to the WRITE_PROTECT register
- 0x40 : Disable all writes except WRITE_PROTECT, OPERATION and PAGE commands
- 0x20 : Disable all writes except WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG and VOUT_COMMAND commands
- 0x00 : Enable writes to all commands

This register is always set to 0x80 (disable all write) at power up.

9.3 STATUS_WORD (Register 0x79)

The STATUS_WORD command returns 2 bytes with a summary of the unit's condition. A value of 1 for the bit indicates a fault or warning event has occurred and a value of 0 indicates a normal event. A read to this status register will clear/deactivate the SMBALERT# (INT) signal.

9.4 STATUS_VOUT (Register 0x7A)

The STATUS_VOUT register returns the condition of the Output Voltage. A value of 1 for the bit indicates a fault or warning event has occurred.

9.5 STATUS_IOUT (Register 0x7B)

The STATUS_IOUT register returns the condition of the Output Current. A value of 1 for the bit indicates a fault or warning event has occurred.

9.6 STATUS_INPUT (Register 0x7C)

The STATUS_INPUT register returns the Input condition. A value of 1 for the bit indicates a fault or warning event has occurred.

9.7 STATUS_TEMPERATURE (Register 0x7D)

The STATUS_TEMPERATURE register returns the thermal condition of the power supply. A value of 1 for the bit indicates a fault or warning event has occurred.

9.8 STATUS_MFR_SPECIFIC (Register 0x80)

The STATUS – MFR_SPECIFIC register indicates the live status of the supply and is not affected by CLEAR_FAULT, removal of the BIAS supply, and will come up displaying the current status of the supply after power cycling.

9.9 STATUS_FAN_1_2 (Register 0x81)

The STATUS_FAN_1_2 register returns the condition of the fans inside the power supply. A value of 1 for the bit indicates a fault or warning event has occurred.

Bits	Description	Operation
0	Input Line Sense	0 = High Line (180 V_{AC} to 264 V_{AC}) / 1 = Low Line (90 V_{AC} to 132 V_{AC})
1	ACOK/INPUTOK	0 = INPUT NOT GOOD / 1 = INPUT OK
2	DCOK	0 = DC NOT OK / 1 = DC OK
3	OVT	0 = Over Temperature / 1 = Temperature OK
4	FAULT	0 = Fault detected / 1 = No Fault
5	OC	0 = Over Current Condition / 1 = No Over Current
6	OVSD	0 = Over Voltage Shutdown / 1 = No Over Voltage
7	DCOK_INT	0 = Output Voltage off limit / 1 = Output Voltage is valid

9.10 USER_DATA_00 & 01 (Registers 0xB0, 0xB1)

The Power Supply provides 96 bytes of EEPROM memory within the microcontroller for the Host System to store information. This command uses BLOCK WRITE and BLOCK READ to store and retrieve information of up to 48 bytes in each of two registers. A delay of 300ms is recommended after each block write.

WARNING: Each write in these registers should be done in 48 byte blocks, else the remaining bytes in memory will be corrupted. In other words, if a write of 8 bytes is done, the other 40 bytes will be corrupted.

9.11 FRW_ VERSION (Register 0xD0)

This register provides the Major Firmware Version (High Nibble) and the Minor Firmware Version (Low Nibble) of the firmware.

9.12 ILIMIT_CTRL_I²C (Register 0xD3)

This register set/read the current limit of the output. The setting cannot be set higher than the default setting (Maximum current limit value – 130% of I_{OUT} Nominal). The user can also set the current limit base on the V_{OUT} reading to create a constant power characteristic on the output. This register is reported in 1/100A as a 16 – bit binary numbers (each least significant bit represents 1/100 A).

9.13 VOUT_CTRL_I²C (Register 0xD4)

This register set/read the voltage setting of the output. This register is set/reported in 1/512V as a 16 – bit binary numbers (each least significant bit represents 1/512V). This register is only active when VProg signal is above 3V or floating.

9.14 FAN_DUTY_CYCLE I²C (Register 0xD6)

This register read the current fan speed in % 100 means full speed.

9.15 FAN_CONTROL I²C (Register 0xD7)

This register read/sets the fan speed setting in % 100 means full speed. The fan speed can only be instructed to spin faster than commanded by the power supply's internal fan control. Setting this register to 0% instructs the power supply to revert back to its internal fan control.

9.16 VPROG_EXT (Register 0xD8)

This register reads the voltage setting at the VPROG_EXT pin from the output connector. The VPROG_EXT register is reported in 3.3/1023 volts as a 16-bit binary numbers (each least significant bit represents ~3.226 mV). The maximum voltage at this pin must be 3.3V.

9.17 READ_VOUT_ I²C (Register 0xE0)

This register provides the measured output voltage of the main output. The output voltage is reported in 1/512 volts as a 16 – bit binary numbers (each least significant bit represents 1/512V).

9.18 READ_IOUT_ I²C (Register 0xE1)

This register provides the measured output current of the main output. The output current is reported in 1/100 amps as a 16 – bit binary numbers (each least significant bit represents 1/100A).

9.19 READ_TS_ I²C (Register 0xE2)

This register provides the internal hotspot temperature of the power supply. The temperature sensor data is reported in °C as a 16 bit signed binary number.

9.20 CMD_OFF_ I²C (Register 0xE3)

This register controls the state of the output.

- 0x0000 = Turn ON the power supply output
- 0x0001 = Turn OFF the power supply output

When the Power Supply is turned ON, all Status registers will be cleared, latch removed, and the SMBALERT# (INT) signal deactivated.

9.21 OTF_LIMIT_ I²C (Register 0xE4)

This register specifies at what temperature the power supply should shutdown in case of over temperature. The register is set in °C as a 16 bit signed number. This register cannot be set higher than the maximum manufacturing value.

9.22 OTF_RECOVERY_ I²C (Register 0xE5)

This register specifies at what temperature the power supply should recover after an over temperature shutdown. The register is set in °C as a 16 bit signed binary number. At least 5°C of hysteresis should be provided between shutdown and recovery.

9.23 DCOKHI_ I²C (Register 0xE6)

This register sets the upper voltage comparison level for the DCOK_INT bit in the STATUS_MFR_SPECIFIC register (0x80) The system controller is capable of changing the default warning level by writing to this register. The register is set/reported in 1/512 volt as a 16 bit number (each least significant bit represents 1/512V).

9.24 DCOKLO (Register 0xE7)

This register sets the lower voltage comparison level for the DCOK_INT bit in the STATUS_MFR_SPECIFIC register (0x80) The system controller is capable of changing the default warning level by writing to this register. The register is set/reported in 1/512 volt as a 16 bit number (each least significant bit represents 1/512V).

9.25 FAN1_SPEED_ I²C (Register 0xE9)

This register provides the measured Fan1 speed. Fan1 speed is reported in RPM as a 16 bit number.

9.26 FAN2_SPEED_ I²C (Register 0xEA)

This register provides the measured Fan2 speed. Fan2 speed is reported in RPM as a 16 bit number.

9.27 VIN_ I²C (Register 0xED)

This register provides the input voltage to the power supply. The input voltage is reported in 1/100v RMS as a 16 bit number.

9.28 IIN_ I²C (Register 0xEE)

This register provides the input current to the power supply. The input current is reported in 1/100A RMS as a 16 bit number.

9.29 PIN_ I²C (Register 0xEF)

This register provides the input power. The input power is reported in watts (W) as a 16 bit number.

10 I²C AND PMBUS REGISTER SET SUMMARY

The digital interface for the Power Supply is fully compliant to PMBus protocol. Manufacturer specific commands (i.e.: I²C commands) located at 0xD0 to 0xEF provide instructions that either do not exist in the general PMBus specification or make the communication interface simpler and more efficient.

10.1 Linear Data Format Definition

The PMBus protocol uses the Linear Data Format definition from Section 7.1 of Part II of the PMBus Power System Mgt Protocol Specification. The exception to this format is the output voltage read function, consistent with the PMBus specification.

The Linear Data Format is a two byte value with an 11 – bit, two's complement mantissa and a 5 – bit, two's complement exponent or scaling factor, its format is shown below.

	Data Byte High								Data Byte Low							
Bit Location	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Exponent (E)					Mantissa (M)										

The relationship between the Mantissa, Exponent, and Actual Value (V) is given by the following equation:

$$V = M * 2^{E}$$

Where:

V is the value
M is the 11 – bit, two's complement mantissa
E is the 5 – bit, two's complement exponent

For more details about PMBus commands, please check PMBus v1.1 specification documents.

Access: RO = Read Only; R/W = Read/Write; Byte order is LSB first

Cmd	Command Name	Type	Bytes	Comments
0x00	PAGE	R/W	1	Not implemented at this time.
0x01	OPERATION	R/W	1	
0x02	ON_OFF_CONFIG	R/W	1	0x09, Output ON at startup
0x03	CLEAR_FAULTS	W	0	Clear SMBALERT signal also
0x10	WRITE_PROTECT	R/W	1	0x80, write protected at power up
0x11	STORE_DEFAULT_ALL	W	0	
0x12	RESTORE_DEFAULT_ALL	W	0	
0x19	CAPABILITY	RO	1	Value:0x30 (400KHz, SMBALERT)
0x20	VOUT_MODE	RO	1	0x17, N=-9, linear mode only, READ ONLY
0x21	VOUT_COMMAND	R/W	2	See specific product's Detailed Specification for value (linear format)
0x3B	FAN_COMMAND_1	R/W	2	In RPM (linear format), Set fan speed
0x40	VOUT_OV_FAULT_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x41	VOUT_OV_FAULT_RESPONSE	R/W	1	See specific product's Detailed Specification for value (linear format)
0x42	VOUT_OV_WARN_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x43	VOUT_UV_WARN_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x44	VOUT_UV_FAULT_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x45	VOUT_UV_FAULT_RESPONSE	R/W	1	See specific product's Detailed Specification for value (linear format)
0x46	IOUT_OC_FAULT_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)

Cmd	Command Name	Type	Bytes	Comments
0x47	IOUT_OC_FAULT_RESPONSE	R/W	1	See specific product's Detailed Specification for value (linear format)
0x4A	IOUT_OC_WARN_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x4F	OT_FAULT_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x50	OT_FAULT_RESPONSE	R/W	1	See specific product's Detailed Specification for value (linear format)
0x51	OT_WARN_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x52	UT_WARN_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x53	UT_FAULT_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x54	UT_FAULT_RESPONSE	R/W	1	See specific product's Detailed Specification for value (linear format)
0x55	VIN_OV_FAULT_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x57	VIN_OV_WARN_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x58	VIN_UV_WARN_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x59	VIN_UV_FAULT_LIMIT	R/W	2	See specific product's Detailed Specification for value (linear format)
0x78	STATUS_BYTE	RO	1	
0x79	STATUS_WORD	RO	2	
0x7A	STATUS_VOUT	RO	1	
0x7B	STATUS_IOUT	RO	1	
0x7C	STATUS_INPUT	RO	1	
0x7D	STATUS_TEMPERATURE	RO	1	
0x7E	STATUS_CML	RO	1	
0x7F	STATUS_OTHER	RO	1	
0x80	STATUS_MFR_SPECIFIC	RO	1	See chapter 5.5.8
0x81	STATUS_FAN_1_2	RO	1	
0x88	READ_VIN	RO	2	(linear format)
0x89	READ_IIN	RO	2	(linear format)
0x8B	READ_VOUT	RO	2	(linear format)
0x8C	READ_IOUT	RO	2	(linear format)
0x8D	READ_TEMPERATURE_1	RO	2	(linear format)
0x90	READ_FAN_SPEED_1	RO	2	In RPM (linear format)
0x91	READ_FAN_SPEED_2	RO	2	In RPM (linear format)
0x96	READ_POUT	RO	2	(linear format)
0x97	READ_PIN	RO	2	(linear format)
0x98	PMBUS_REVISION	RO	1	0x11
0x99	MFR_ID	RO	5	Read only (Write protected)
0x9A	MFR_MODEL	RO	15	Read only (Write protected)
0x9B	MFR_REVISION	RO	4	Read only (Write protected)
0x9C	MFR_LOCATION	RO	4	Read only (Write protected)
0x9D	MFR_DATE	RO	6	Read only (Write protected)
0x9E	MFR_SERIAL	RO	15	Read only (Write protected)
0xA0	MFR_VIN_MIN	RO	2	See specific product's Detailed Specification for value (linear format)
0xA1	MFR_VIN_MAX	RO	2	See specific product's Detailed Specification for value (linear format)
0xA2	MFR_IIN_MAX	RO	2	See specific product's Detailed Specification for value (linear format)

Cmd	Command Name	Type	Bytes	Comments
0xA3	MFR_PIN_MAX	RO	2	See specific product's Detailed Specification for value (linear format)
0xA4	MFR_VOUT_MIN	RO	2	See specific product's Detailed Specification for value (linear format)
0xA5	MFR_VOUT_MAX	RO	2	See specific product's Detailed Specification for value (linear format)
0xA6	MFR_IOUT_MAX	RO	2	See specific product's Detailed Specification for value (linear format)
0xA7	MFR_POUT_MAX	RO	2	See specific product's Detailed Specification for value (linear format)
0xA8	MFR_TAMBIENT_MAX	RO	2	See specific product's Detailed Specification for value (linear format)
0xA9	MFR_TAMBIENT_MIN	RO	2	See specific product's Detailed Specification for value (linear format)
0xB0	USER_DATA_00	R/W	48	No offset (write/read in 48 bytes block), (Block Read/Write format), see Section 7 above.
0xB1	USER_DATA_01	R/W	48	No offset (write/read in 48 bytes block), (Block Read/Write format), see Section 7 above.
	OmniOn-Energy_I²C command (0xD0 to 0xEF), see chapter 5.5 for more details			
0xD0	FRW_REVISION	RO	1	
0xD1	Reserved			
0xD2	Reserved			
0xD3	ILIMIT_CTRL_I²C	R/W	2	Current Limit Setting (1/100A)
0xD4	VOUT_CTRL_I²C	R/W	2	Output Voltage Setting (1/512V)
0xD5	VOUT_OFFSET	R/W	1	Offset for Vout reading
0xD6	FAN_DUTY_CYCLE_I²C	RO	1	Read fan duty cycle (0 to 100%)
0xD7	FAN_CONTROL_I²C	R/W	1	Set fan speed in duty cycle (0 to 100%)
0xD8	VPROG_EXT	RO	2	VPROG signal value (3.3/1023 volt)
0xD9	Reserved for OmniOn Energy			
0xDA	Reserved for OmniOn Energy			
0xDB	Reserved for OmniOn Energy			
0xDC	Reserved for OmniOn Energy			
0xDD	Reserved for OmniOn Energy			
0xDE	Reserved for OmniOn Energy			
0xDF	Reserved for OmniOn Energy			
0xE0	READ_VOUT_I²C	RO	2	Output Voltage (1/512V)
0xE1	READ_IOUT_I²C	RO	2	Output Current (1/100A)
0xE2	READ_TS_I²C	RO	2	Heat Sink Temperature (°C)
0xE3	CMD_OFF_I²C	RW	2	0: Turn ON, 1: Turn OFF power supply
0xE4	OTF_LIMIT_I²C	RW	2	Over Temperature limit_I²C (°C)
0xE5	OTF_RECOVERY_I²C	RW	2	Over Temperature Recovery_I²C (°C)
0xE6	DCOKHI_I²C	RW	2	High Output Voltage Limit _I²C (1/512V)
0xE7	DCOKLO_I²C	RW	2	Low Output Voltage Limit _I²C (1/512V)
0xE8	Reserved			Reserved
0xE9	FAN 1_SPEED_I²C	RO	2	Fan 1 speed (RPM)
0xEA	FAN 2_SPEED_I²C	RO	2	Fan 2 speed (RPM)
0xEB	Reserved			
0xEC	Reserved			
0xED	VIN_I²C	RO	2	Input Voltage (1/100V)
0xEE	IIN_I²C	RO	2	Input Current (1/100A)
0xEF	PIN_I²C	RO	2	Input Power (W)

Notes:

1. Please refer to PMBus specification Rev 1.1 for more details on PMBus commands.
2. The linear format is only appropriate for PMBus commands.
3. Commands with more than 2 bytes of Data use Block Read/Write format

11 Lack of Command Support

Commands or Sensor Readings that are not supported by a specific CAR module may be listed in that module.

Following the PMBus standard, any command that is not supported is properly identified by setting the CML fault bit in the STATUS_WORD register in conjunction with setting the Invalid/Unsupported Command in the CML register and issuing an SMBAlert# signal.

12 I/O Expander option (PCF8574ATD-T)

Some of the earlier vintage of CAR power supplies, such as the CAR1212FPx, use only an I/O Expander without extended I²C communications (blank under the software option). This I/O Expander has a single status/control byte that is accessible via the default address documented in the individual specifications.

This byte takes the form;

7	6	5	4	3	2	1	0
n/s	n/s	Fault	ON/OFF	Temp_OK	n/s	DCOK	ACOK

n/s – not supported

- Bits 0, 1, 3, and 5 are 'read_only' and are HI [1] during normal operation. The rectifier needs to be biased externally in order to 'read' its operational state without the presence of input power.
- Bit 4 is a 'read/write' bit that can be used to verify the ON/OFF commanded state or change the commanded output of the rectifier. In order to turn the output OFF this bit needs to be pulled LO [0].
- No PEC support is provided. Standard i²c commands apply.

Change History (excludes grammar & clarifications)

Revision	Description	Date/Dept./Init
X08	Updated as per ABB template	November 02, 2022
8.1	Updated as per OmniOn template	November 07, 2023

OmniOn Power Inc.
601 Shiloh Rd.
Plano, TX USA

omnionpower.com