Powering Xilinx™ Kintex® UltraScale+™

Reference Design for Kintex® XCKU15P

Introduction

This reference design provides a solution to power Kintex® XCKU15P based applications. Using ABB Power Modules ensures a dense, high performance and a cost-effective short design time cycle. ABB Power Modules are designed and tested to comply with IPC9592 standards and have millions of hours of Field Reliability

Features

- Digital interface through the PMBus™ protocol
- Tunable Loop™ to optimize dynamic output voltage response
- Fixed switching frequency with capability of external synchronization
- Output over current protection (non-latching)
- Over temperature protection
- Remote On/Off
- *UL** 60950-1 2nd Ed. Recognized, *CSA*† C22.2 No. 60950-1-07 Certified, and *VDE*‡ (EN60950-1 2nd Ed.) Licensed

Applications

- NIC Cards
- Data accelerator

Powertree

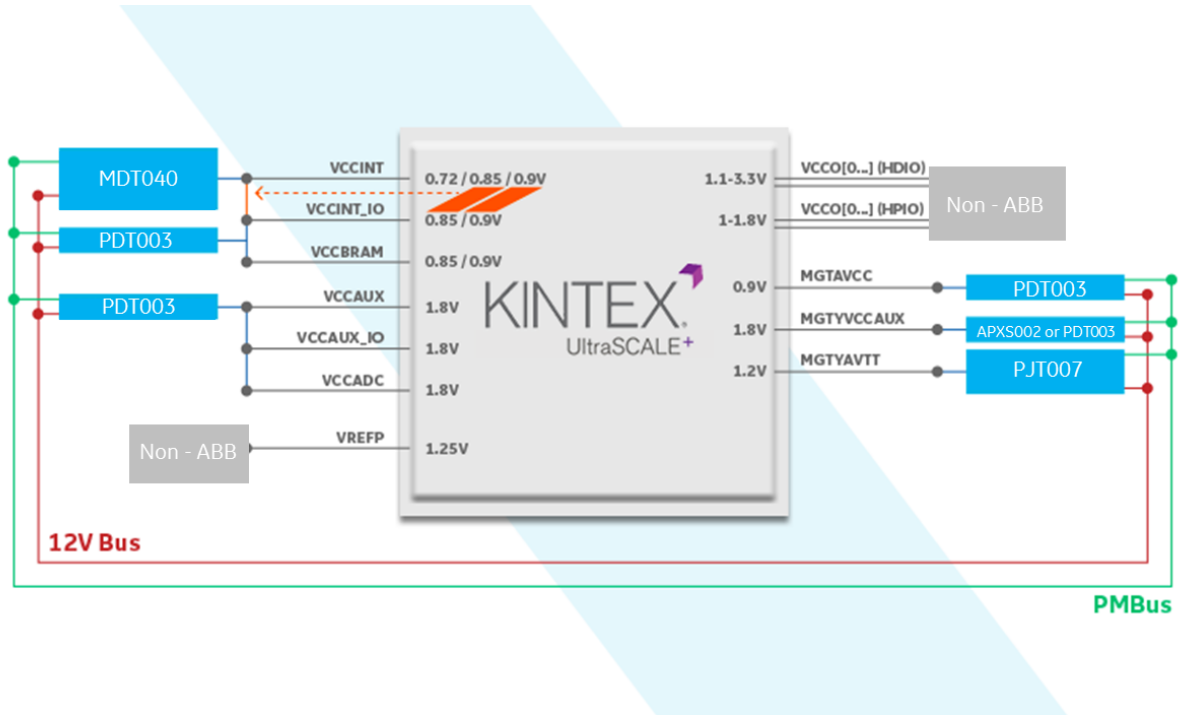

Figure 1 – ABB Module Solution for key power rails for XCKU15P configuration based on Upper Load Consumption

XCKU15 Power Rail and ABB Module Specifications

RAIL	VOLTAGE	ABB MODULE	MODULE OUTPUT	COMMENTS
VCCINT	0.72/0.85/0.9V, ±3%	MDT040	40A	SETPOINT ±1%, Balance Load Step + Ripple + Regulation
VCCBRAM/INT_IO	0.85/0.9V, ±3%	PDT003	3A	SETPOINT ±1%, Balance Load Step + Ripple + Regulation. Rail can be tied to VCCINT if both set to same voltage.
VCCAUX/ADC	1.8V, ±3%	PDT003	3A	SETPOINT ±1%, Balance Load Step + Ripple + Regulation
VMGTAVTT	1.2V, ±3%	PJT007	7A	SETPOINT ±0.5%, Balance Load Step + Ripple + Regulation, <10mV pk-pk ripple
VMGTVCCAUX	1.8V, ±3%	APXS002 or PDT003	2A / 3A	SETPOINT ±1%, Balance Load Step + Ripple + Regulation, <10mV pk-pk ripple
VMGTAVCC	0.9V, ±3%	PDT003	3A	SETPOINT ±1%, Balance Load Step + Ripple + Regulation, <10mV pk-pk ripple

ABB Reference Solutions

ABB's products used in these reference designs are fully integrated Point-of-Load power modules providing a high reliability (IPC9592 qualified), easy-to-use, fast time-to-market, high efficiency, small footprint, and excellent thermal derating option for powering FPGAs. ABB's reference designs use digital power modules with PMBus™ making sequencing easy. Reference designs do not include a power management IC but any external PMBus compliant controller or the external I2C/PMBus based system controller can be used to sequence and monitor the rails

ABB Module Description

MDT040 – The MDT040 is a dense single phase Buck Converter with PMBus communications support for start-up and sequencing control. This high-power, full-featured module operates from 4.5-14.4 Vin and provides an output of 40A over an adjustable output voltage range of 0.45 to 2.0Vdc. It has low output noise and offers Tunable Loop Control for tight load response. It is compliant to Category 2 of IPC-9592. Detailed Datasheet available at **https://www.geindustrial.com/products/embedded-power/dlynx**

PJT007 – The PJT007 provides 7A of output in a DOSA compliant PICO footprint. This single-phase Buck Converter operates from 4.5 -14.4 Vin and provides an output of 7A over an adjustable output voltage range of 0.51 to 5.5Vdc. It has a PMBus interface for start-up and sequencing control; and Tunable Loop™ to ensure a tight load transient performance. It is compliant to Category 2 of IPC-9592. Detailed Datasheet available at https://www.geindustrial.com/products/embedded-power/dlynx-ii

PDT003 – The PDT003 provides 3A of output in a DOSA compliant PICO footprint. This single-phase Buck Converter operates from a wide 3 -14.4 Vin and provides an output of 3A over an adjustable output voltage range of 0.45 to 5.5Vdc. It has a PMBus interface for on/off control; and Tunable Loop™ to ensure a tight load transient performance. It is compliant to Category 2 of IPC-9592. Detailed Datasheet available at https://www.geindustrial.com/products/embedded-power/dlynx

APXS002 – The APXS002 provides 2A of output in a DOSA compliant PICO footprint. This single-phase Buck Converter operates from a wide 3 -14Vin and provides an output of 2A over an adjustable output voltage range of 0.6 to 5.5Vdc. It has an analog interface for on/off control; and Tunable Loop™ to ensure a tight load transient performance. It is a cost-effective solution where digital communication is not required or is not available. Detailed Datasheet available at https://www.geindustrial.com/products/embedded-power/tlynx

Hardware for Testing

The main hardware used was the XCKU15P evaluation board and associated test equipment

Figure 2 – Evaluation Board Top and Bottom View

Test Equipment

Function	Make	Model
DC Power Supply	Chroma	62050P-100-100
DC Load 1	Chroma	63205A-150-500
DC Load 2	Agilent	N3300A
Oscilloscope	Teledyne Lecroy	HDO6104
Scope Probe (Voltage)	HP	10070A
Scope Probe (Current)	Teledyne Lecroy	AP015
Function Generator	Agilent	22310A
Bode Plots	Venable	Model 350 system

Tests

Module Output On-Off Sequencing

Module output was turned on and off using PMBus for those rails that needed a specific sequencing order as specified in the Xilinx™ documentation. An external computer running ABBs DPI-ProGUI software was used to turn on modules in sequence. A free version of the software is available here http://go.ge-energy.com/DigitalPowerInsight.html

Efficiency

Module Efficiency was measured on individual evaluation boards which provided better access to individual module input and output points to get an accurate readback of efficiency. Efficiency curves have been generated from fixed measurements at standard interval point through a standardized test equipment setup and then data interpolated to provide the efficiency at specific output voltages.

Output Ripple Voltage

The Output Ripple Voltage was measured using Tektronics probe connector (Part No 131-4353-00) mounted close to the load terminations on the evaluation board. Measurements were done for the upper load specified by Xilinx™ for each rail in the XCKU15P configuration.

Load Transient

For the VCCINT rail a simple power FET circuit was added to the evaluation board to generate the fast rise time demanded by the rail. The output voltage was measured at the same point where the

output ripple was measured. For other rails the a short connection to the Chroma Load was made to enable the appropriate step load and slew rate for each rail.

Bode Plots

Loop Gain Measurements were done on the individual rails at upper load levels specified by Xilinx™

Load Regulation

Measurement at the load of the variation in output voltage with Sense Line from modules connected to the Output Load

Thermal

A Thermal image using an IR Camera was captured of the board after running all the modules on the board at Xilinx specified upper load for each rail for 20 minutes.

Module Output On-Off Sequencing Curves

Figure 3 – ON Sequence – VCCINT (Yellow), VCCBRAM(Red), VCCAUX(Blue) (Axis Scale : 500mV(y), 1s(x))

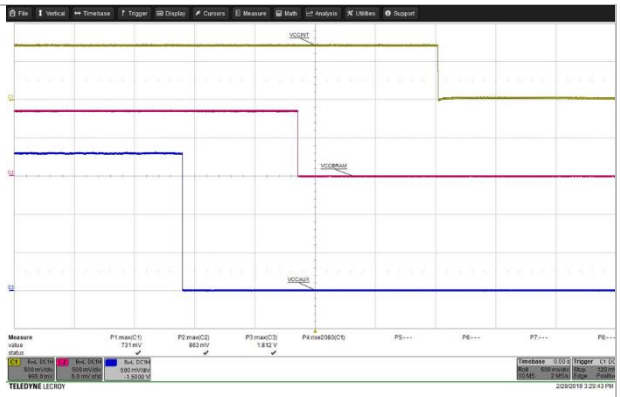

Figure 4 – OFF Sequence – VCCINT (Yellow), VCCBRAM(Red), VCCAUX(Blue) (Axis Scale : 500mV(y), 500ms(x))

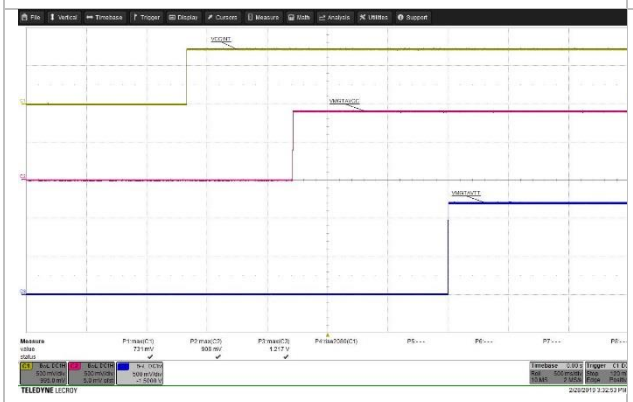

Figure 5 – ON Sequence – VCCINT (Yellow), VMGTAVCC(Red), VMGTAVTT(Blue) (Axis Scale :500mV(y), 500ms(x))

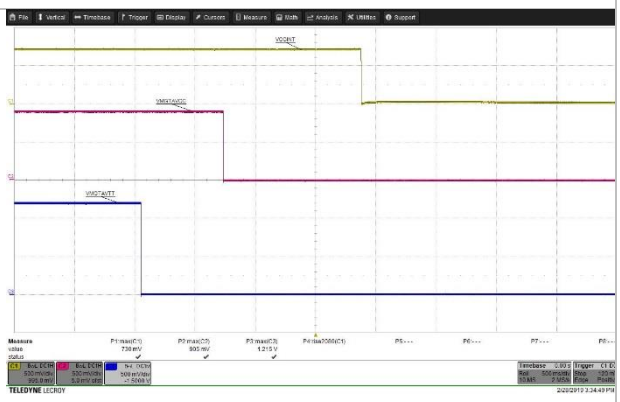

Figure 6 – OFF Sequence – VCCINT (Yellow), VMGTAVCC(Red), VMGTAVTT(Blue) (Axis Scale :500mV(y), 500ms(x))

Note: For full-size plots, download complete report. Go to Test Report.

Efficiency Curves

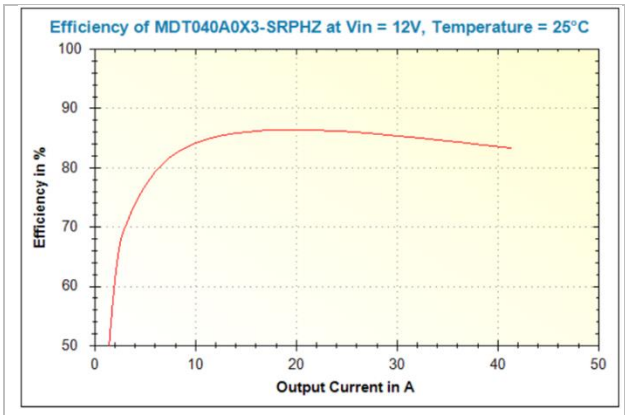

Figure 7 – VCCINT Efficiency – MDT040 (0.72Vout)

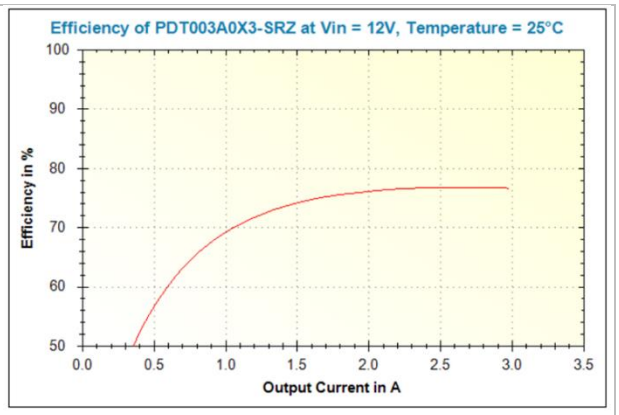

Figure 8 – VCCBRAM/IO Efficiency – PDT003 (0.85Vout)

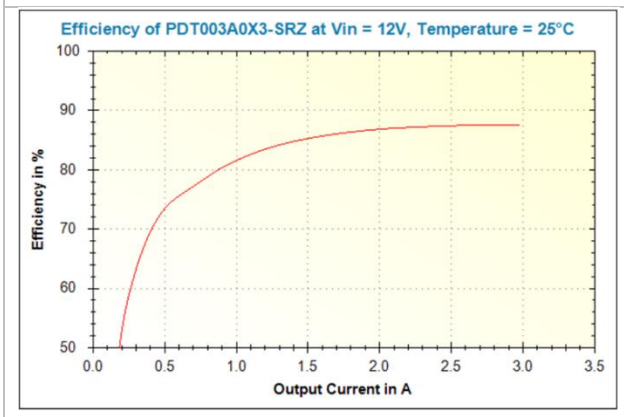

Figure 9 – VCCAUX Efficiency – PDT003 (1.8Vout)

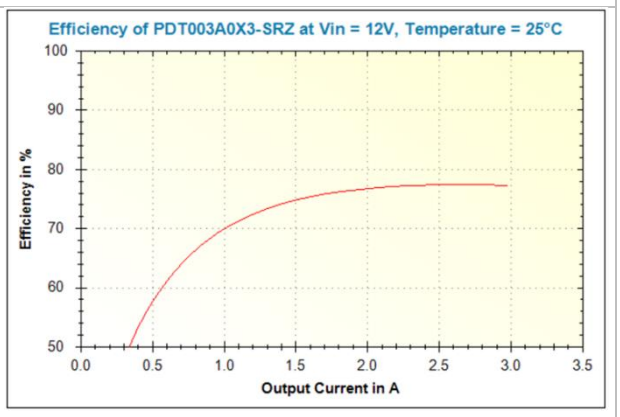

Figure 10 – VMGTAVCC Efficiency – PDT003 (0.9Vout)

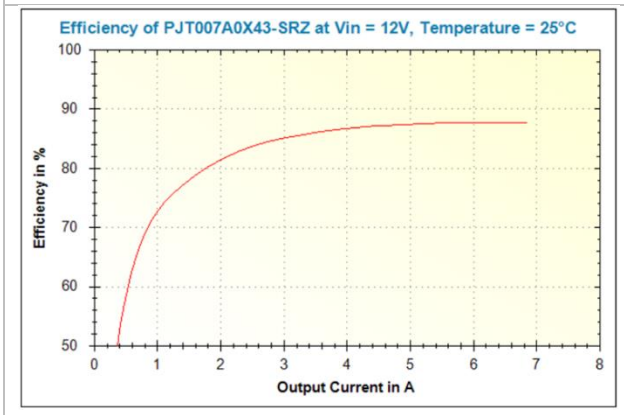

Figure 11 – VMGTAVTT Efficiency – PJT007 (1.2Vout)

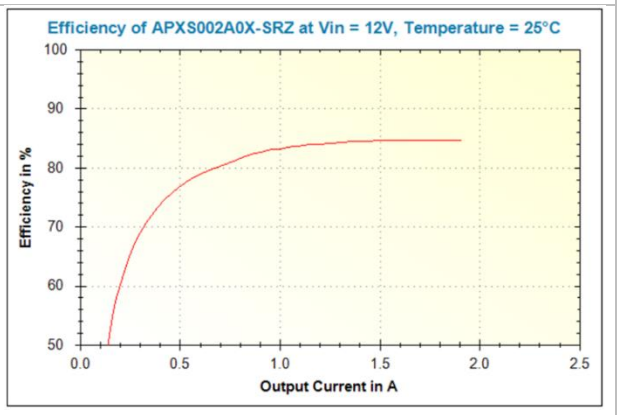

Figure 12 – VMGTVCCAUX Efficiency – APXS002 (1.2Vout)

Output Ripple – All measurements at Upper Load specified by XILINX™

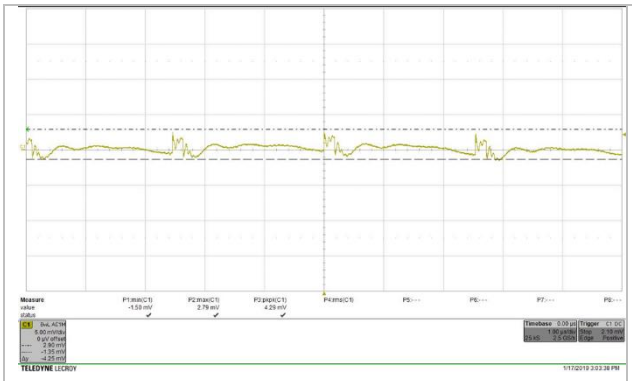

Figure 13–VCCINT–MDT040 (Axis Scale -5mV(y), 1us(x))

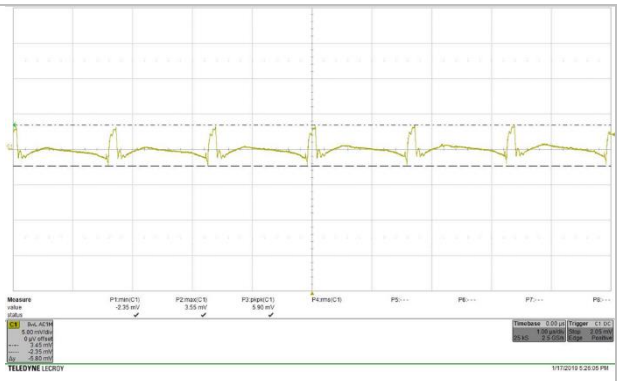

Figure 14–VCCBRAM/IO–PDT003 (Axis Scale 5mV(y), 1us(x))

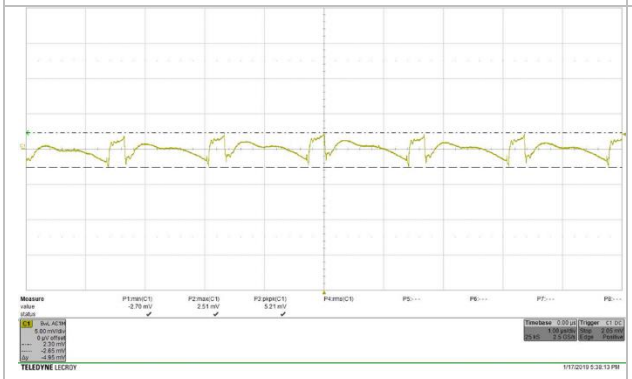

Figure 15–VCCAUX–PDT003 (Axis Scale (5mV(y), 1us(x))

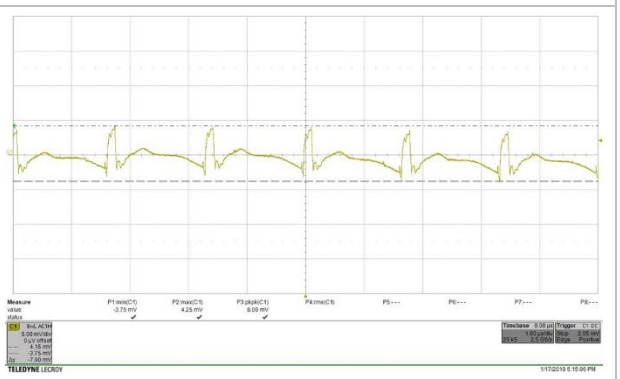

Figure 16–VMGTAVCC–PDT003 (Axis Scale (10mV(y), 1us(x))

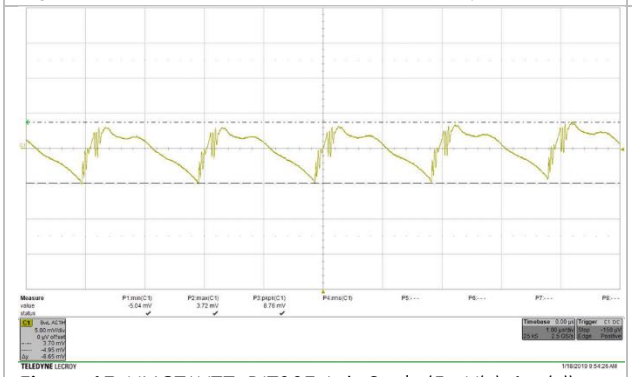

Figure 17–VMGTAVTT–PJT007 Axis Scale (5mV(y), 1us(x))

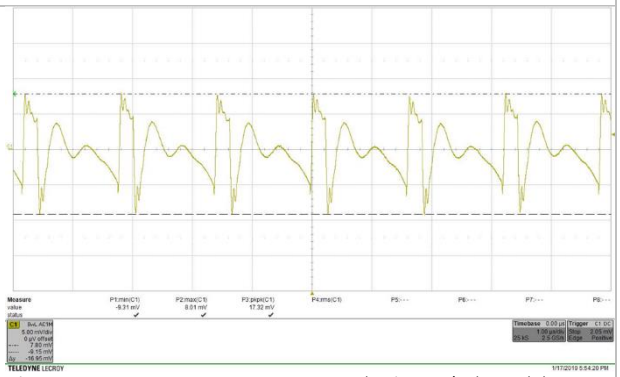

Figure 18–VMGTVCCAUX–APXS002 (Axis Scale (5mV(y), 1us(x))

Transients –

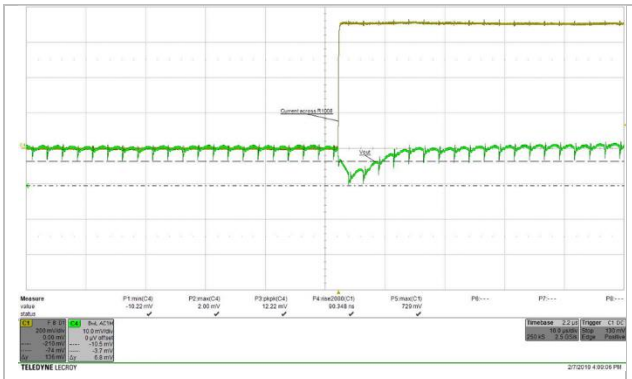

Figure 19 – VCCINT – MDT040 (0.72Vout)

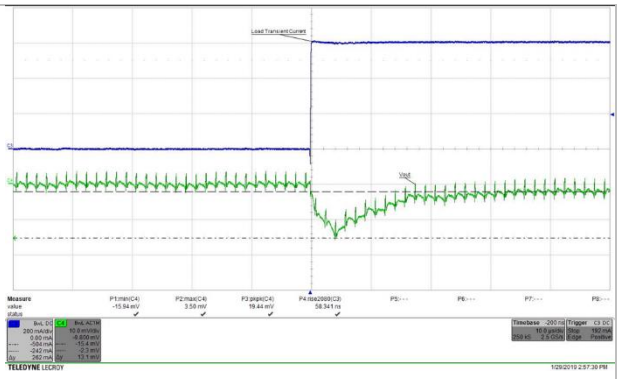

Figure 20– VCCBRAM/IO – PDT003 (0.85Vout)

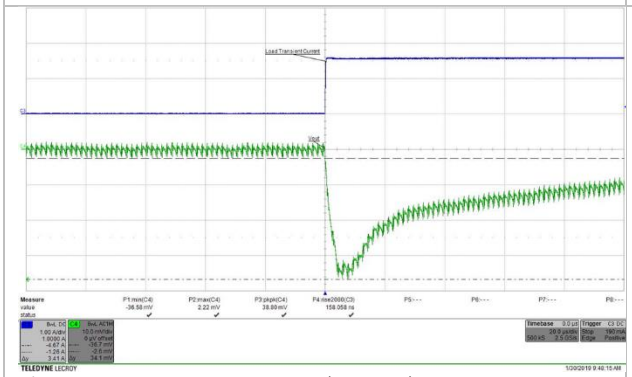

Figure 21 – VCCAUX – PDT003 (1.8Vout)

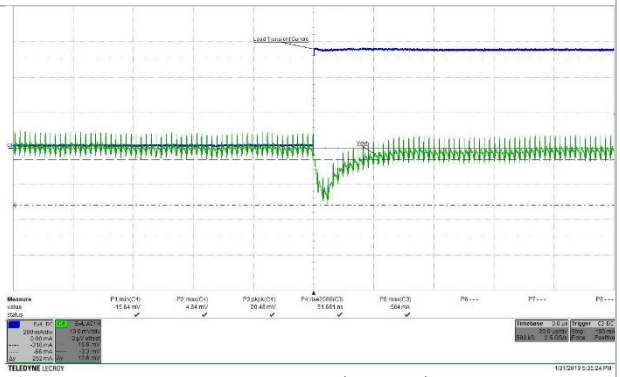

Figure 22 – VMGTAVCC – PDT003 (0.9Vout)

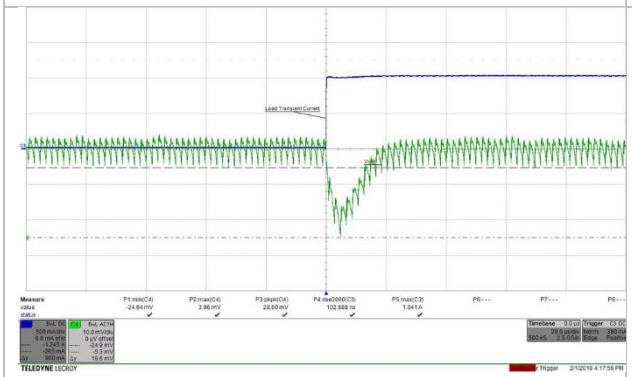

Figure 23 – VMGTAVTT – PJT007 (1.2Vout)

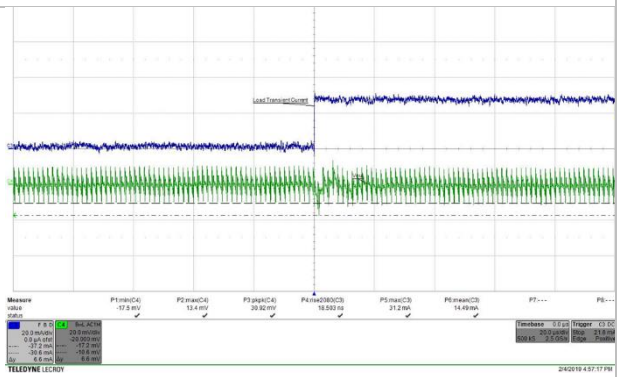

Figure 24 – VMGTVCCAUX – APXS002 (1.2Vout

Note: For full-size plots, download complete report. Go to Test Report.

Bode Plots

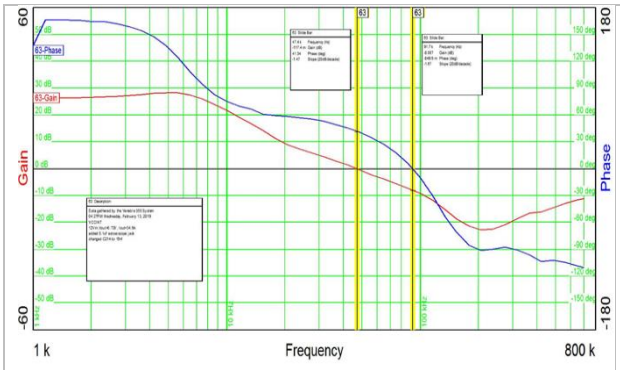

Fig. 25 – VCCINT, MDT040 (0.72Vout), 47kHz BW, 41°PM

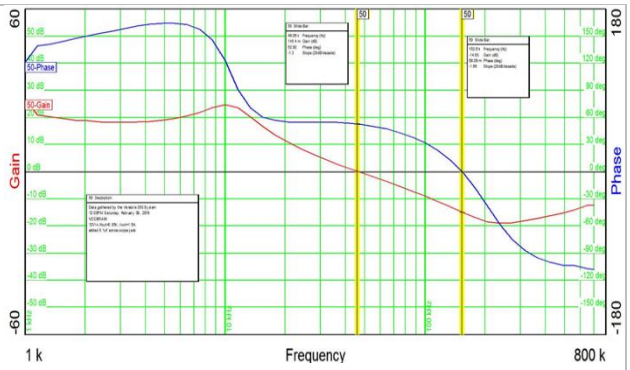

Fig. 26: VCCBRAM/IO, PDT003 (0.85Vo), 46kHz BW, 52°PM

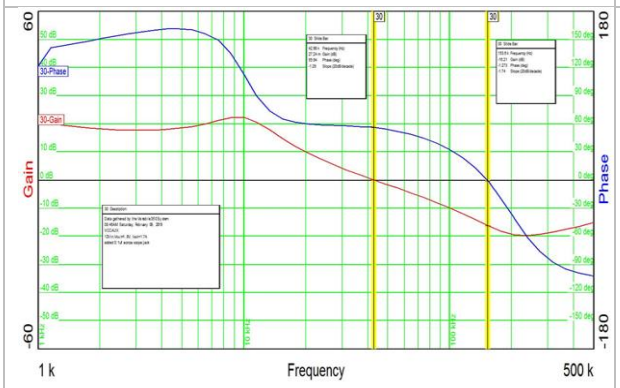

Fig. 27 – VCCAUX – PDT003 (1.8Vo), 43kHz BW, 56°PM

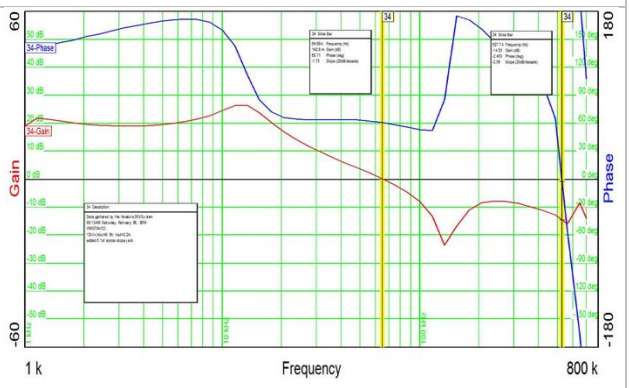

Fig. 28 – VMGTAVCC – PDT003 (0.9Vo) 65kHz BW, 61°PM

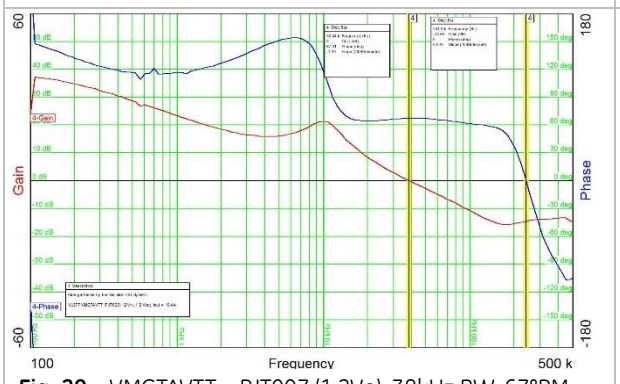

Fig. 29 – VMGTAVTT – PJT007 (1.2Vo), 38kHz BW, 67°PM

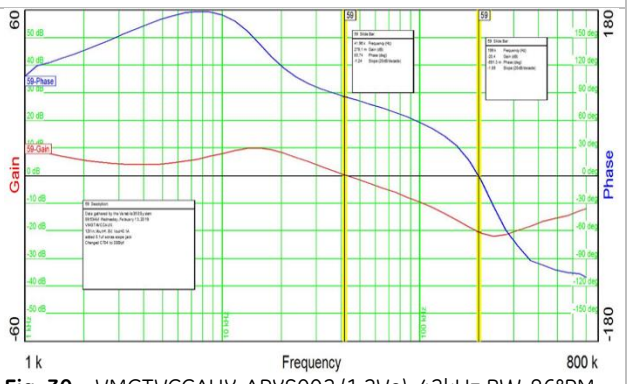

Fig. 30 – VMGTVCCAUX-APXS002 (1.2Vo), 42kHz BW, 86°PM

Note: For full-size plots, download complete report. Go to Test Report.

Load Regulation – All measurements at 12Vin, Upper Load

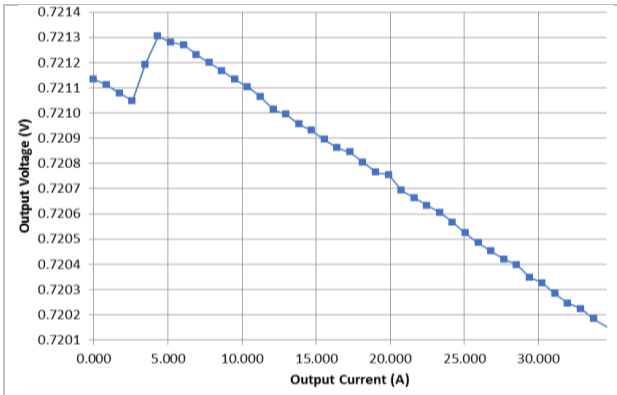

Figure 31: VCCINT – MDT040 (0.72Vout), Δ = 1mV

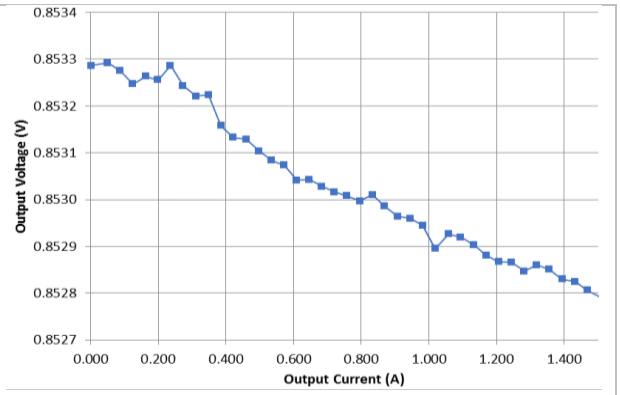

Figure 32: VCCBRAM/IO – PDT003 (0.85Vout), Δ = **0.5**mV

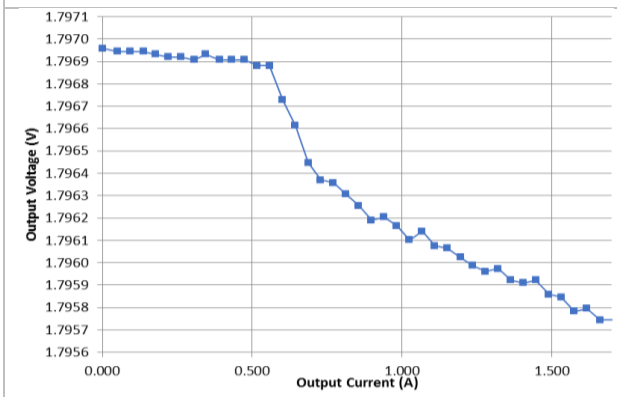

Figure 33: VCCAUX – PDT003 (1.8Vout), Δ = **1.2**mV

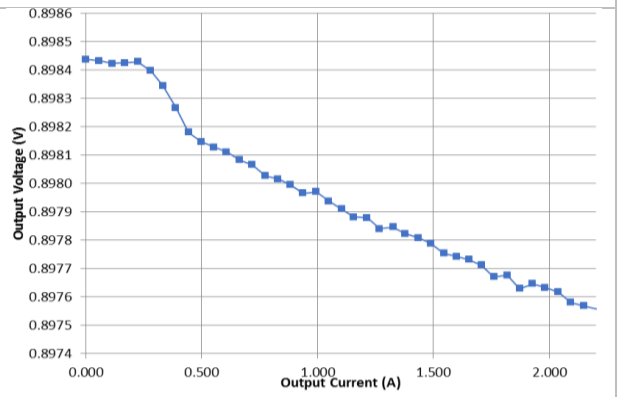

Figure 34: VMGTAVCC – PDT003 (0.9Vout), Δ = **0.9**mV

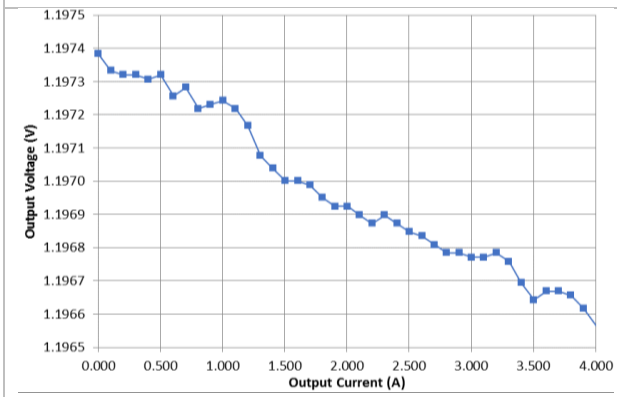

Figure 35: VMGTAVTT – PJT007 (1.2Vout), Δ = 0.83mV

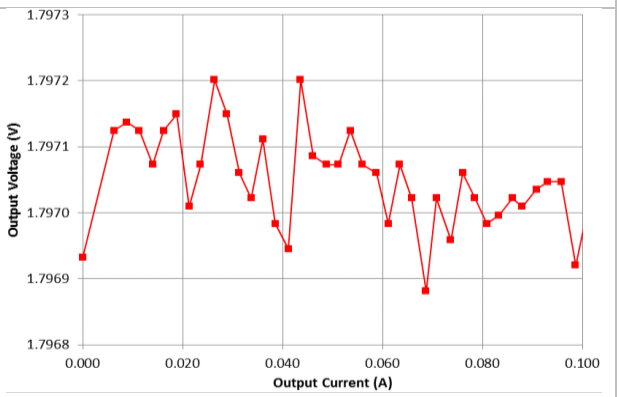

Figure 36: VMGTVCCAUX – APXS002 (1.2Vo), Δ = **0.27**mV

Note: For full-size plots, download complete report. Go to Test Report.

Thermal Image

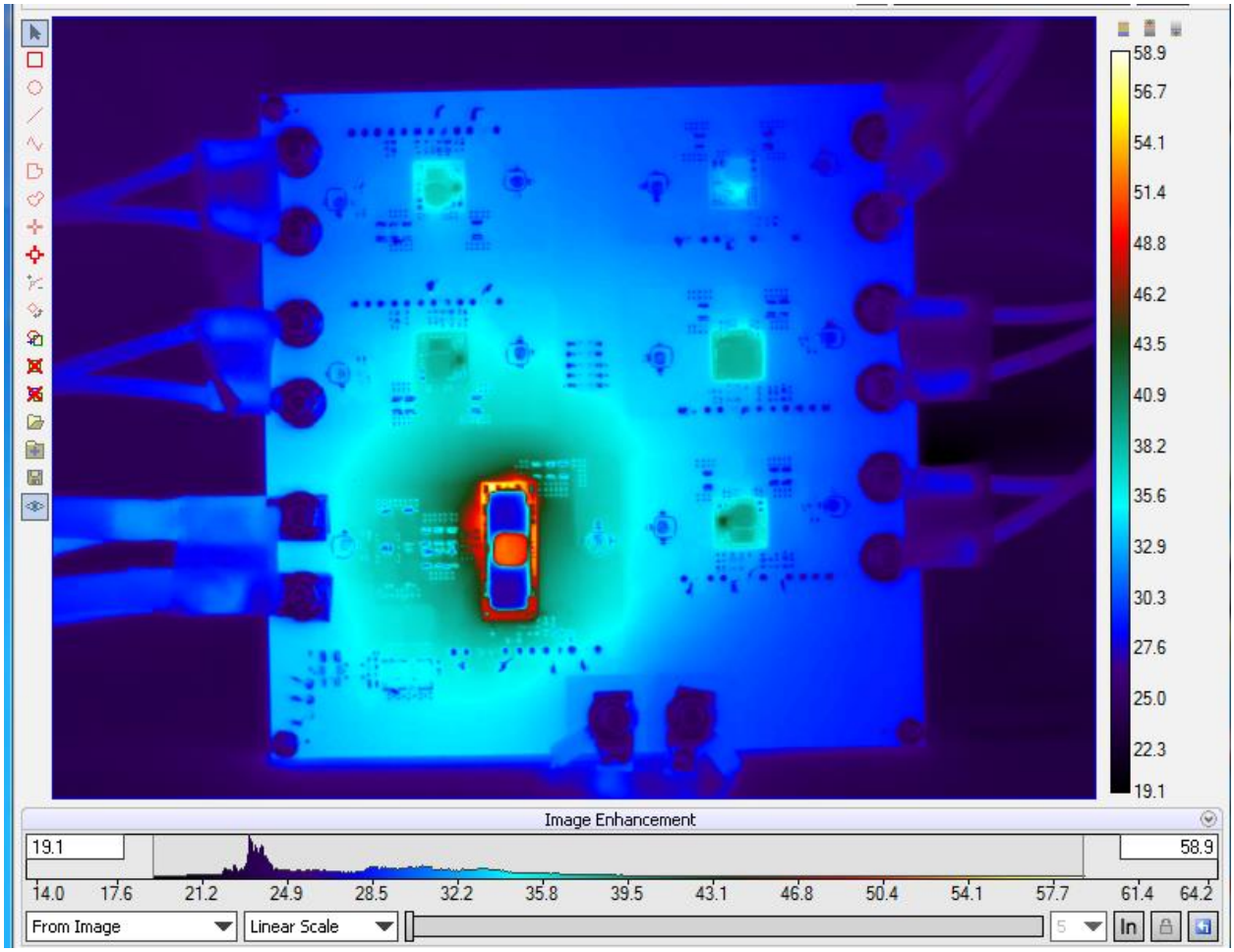

Figure 47 – Thermal image of the board after running all the modules on the board at full load for 20 minutes. Captured using an IR camera.

Design Files and Reference Data

Schematics

To download the schematics, use the following link XCKU15P Schematic.

Bill of Materials

To download the bill of materials (BOM), use the following link XCKU15P BOM.

Evaluation Board Layout

Xilinx has specific instructions in their FPGA Layout guidelines. To download the Layout used on the evaluation board use the following link XCKU15P Layout.

Guidelines for Layout of all ABB DLynx and DLynxII modules are available here: Module Lay-out.

Complete Test Report

Detailed Test Report of testing of ABB Modules on Xilinx Evaluation Board is available. Go to Test Report.

Online Simulation Tool

ABB provides a free, cloud-based simulation tool. Reference Designs in this document are available for simulation. Go to Power Module Wizard.

PMBus Tool and GUI

ABB provides a free downloadable GUI which works with the ABB USB to I2C adapter to allow users to command and monitor ABB Modules. Go to Digital Power Insight.

OnLine Materials

Detailed Datasheet of modules used in this reference design and other Reference Material is available at ABB Modules.